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MICROELECTRONICS INTERCONNECT GROUP INTERCONNECTION SYSTEMS DIVISION		TEST REQUEST NUMBER	

SOLDERCOLUMNS CCMD TEST REPORT ON SERIAL THERMAL CYCLE, SHOCK AND VIBRATION TESTS

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1.0 Introduction

Surface-mounting electronic components directly on Printed Wiring Boards (PWB's) offers several significant advantages over traditional through-hole mounting techniques. These advantages include higher interconnect density and the potential for virtually total automatic component placement, which is attended by lower assembly cost and higher overall reliability.

Widespread adoption of surface-mounting techniques has been hindered by problems arising from the very different demands placed on component mounting techniques [1]. In surface-mounting, the solder joint must act as a structural as well as an electrical interconnecting member.

For materials with widely differing Thermal Coefficients of Expansion (TCE), temperature variations due to environmental changes or power cycling induce strains which jeopardize the solder joint integrity. In the extreme case of a ceramic chip carrier mounted on a glass-epoxy PWB, the TCE mismatch-induced strains often leads to early electrical failure in temperature-cycle testing.

For applications requiring high reliability and long assembly lifetimes, such as for mainframe computers, telecommunications or specialized military systems, there is a need to extend the operating life of high I/O ceramic packages on standard PWB's.

The packaging material of choice for microelectronic components in the market described above is alumina, because of hermiticity, high thermal conductivity, availablilty and cost. Glass-epoxy PWB's are also preferred because of cost, availability and the base of expertise in through-hole board fabrication.

Introduction of compliant leads between the ceramic package and the organic substrate is one way to enable long operating lifetimes of electronic assemblies. This test report details the performance of Raychem's SolderColumnsTM Chip Carrier Mounting Device (CCMD) compliant leads which significantly extend operating lifetimes of these assemblies when compared to conventional direct surface mounting.

2.0 Product Description

Individual columns of the Raychem SolderColumns Chip Carrier Mounting Device are composed of a high melting point solder core with a copper outer spiral for reinforcement. The reinforced solder column also has a thin coating of lower melting point eutectic Sn63-Pb37 solder. Figure 2-1 is a photograph showing columns installed between a Leadless Ceramic Chip Carrier (LCCC) and a Printed Wiring Board (PWB).

Introduction of Raychem SolderColumns CCMD was predicated upon reducing the strain conditions imposed upon the solder joints at the package and PWB surfaces. By separating the package and substrate with compliant columns, lap shear stresses are effectively converted to more benign bending stresses. The reduction in strain results in significantly enhanced component operating life [2].

CCMD columns are provided in two standard outer diameters; .022 inches, used primarily for .050-inch pad spacing, and .015 inches, used primarily for .040-inch pad spacing. Standard lengths are .100 inches and .050 inches, although other lengths are possible.

A typical application of CCMD is in post-leading JEDEC standard LCCC's. Post-leading refers to attachment of package leads after handling associated with micro-component bonding, connection, lid-attach and testing, but before mounting to the assembly substrate.

Use of CCMD in this manner minimizes exposure of package leads to handling, thereby improving the reliability of board-level attachment. Another characteristic of the columns is a high degree of lead end co-planarity, due to compression of the column solder core during the package post-leading operation.

Application of the CCMD is accomplished in a simple operation described in Appendix A using an alignment fixture and some means of solder reflow, such as vapor-phase or infra-red. Handling and board-mounting the post-leaded component thereafter follows conventional surface-mounting techniques.

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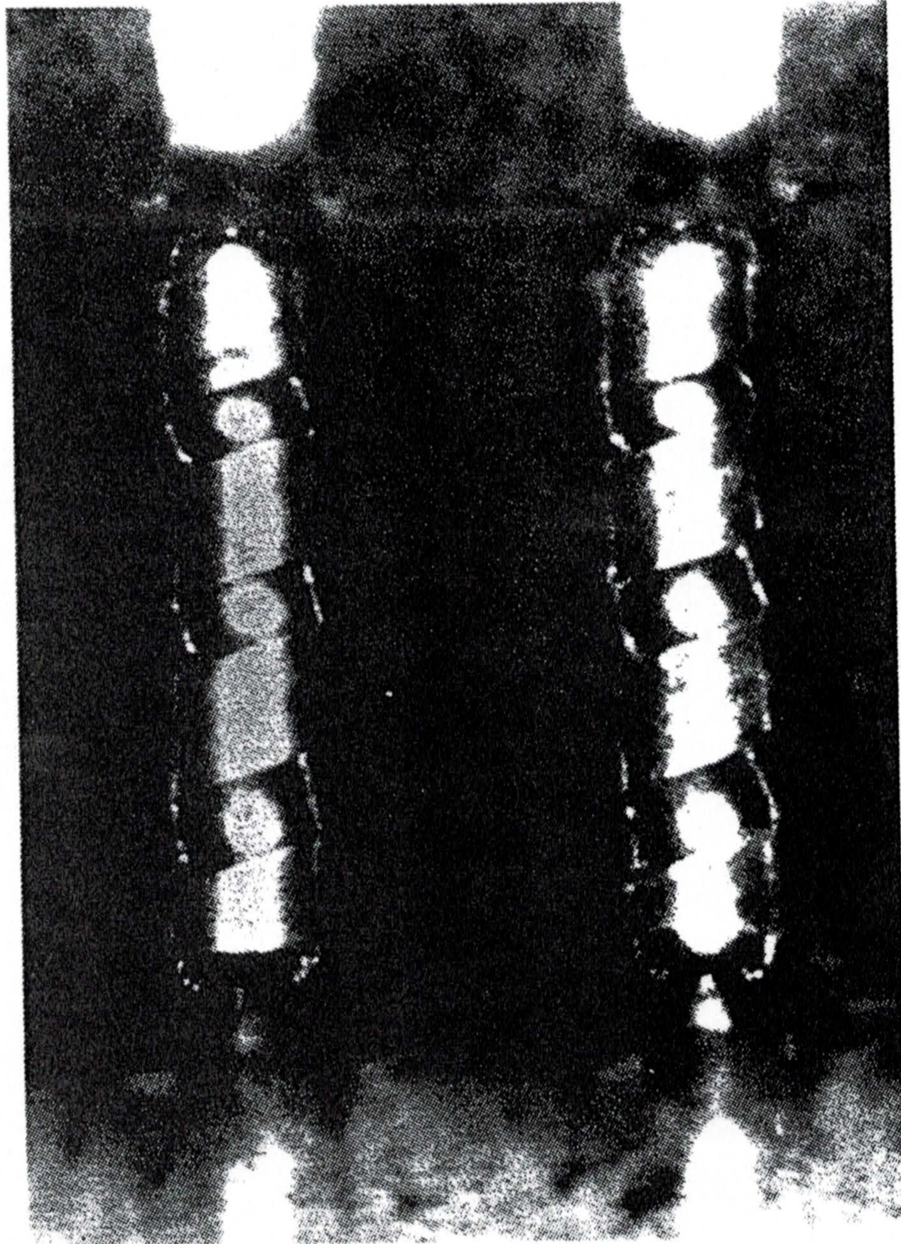

FIGURE 2-1. RAYCHEM SOLDERCOLUMS CCMD, COLUMN DIAMETER .022 INCHES, COLUMN HEIGHT .100 INCHES

3.0 Test Program

3.1 Purpose

The program described in this report was intended to test survivability of assemblies joined using Raychem CCMD's under conditions of sequential temperature-cycle, shock and vibration.

3.2 Scope

Representative test vehicles were subjected to combined stress conditions which might be used to qualify high-reliability components in state-of-the-art electronic systems. The tests were applied in adherence to military and Federal specifications.

3.3 Test Vehicles

Samples were fabricated using JEDEC Type C three-layer 52 I/O LCCC's obtained from GE Ceramics and a 4 X 4.5-inch glass-epoxy single-layer test board 1/16-inch thick with solder-plated copper traces on both sides. LCCC's were joined to the test board with CCMD columns .022 inches in diameter and .050 inches high. A typical sample is shown in Figure 3-1.

Conductive traces on the PWB were arranged to form a test loop so the resistance of each individual column could be measured from pads along the card edge using a four-probe technique. A schematic of a test loop, including PWB traces, column with end fillets and wiring around the periphery of the LCCC, is shown in Figure 3-2. The resistance is calculated only for the portion of the loop between points A and B.

3.4 Failure

During testing, the samples were periodically placed in a device which automatically recorded the resistance of the test loop segment between points A and B in Figure 3-2. It was assumed that any change in the resistance value was attributable to degradation of the column and its end fillets. A column was presumed to fail electrically when an increase of 30 milliohms or more was registered relative to the initial resistance. A typical resistance reading before testing began was 3-6 milliohms. The 30 milliohm relative increase criterion was considered a reasonable choice among the several in use for testing in the industry [3,4].

In addition to electrical probing, each Soldercolumn was visually inspected at 25X before and after a test series. Failure of a Soldercolumn was presumed if any column was observed to have failed mechanically.

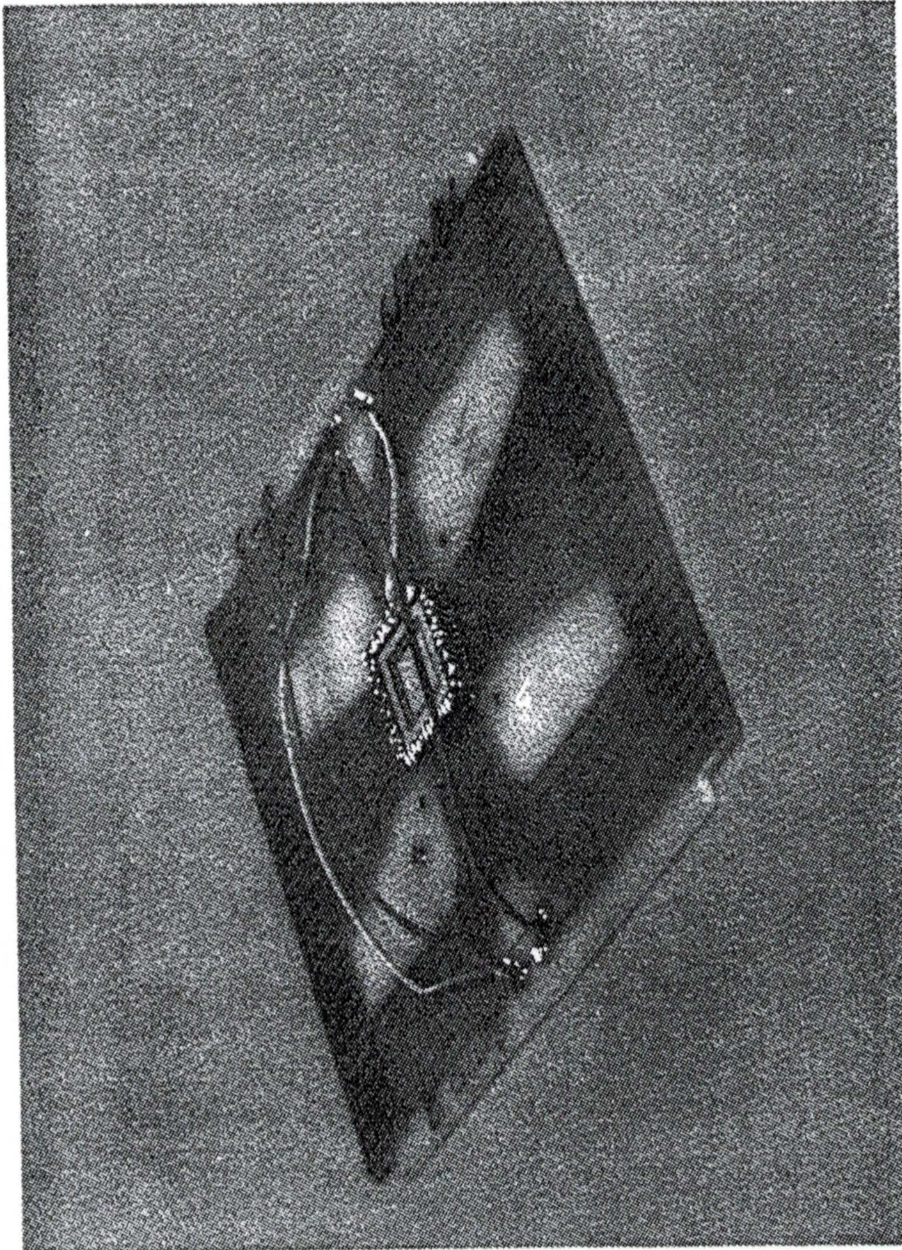

FIGURE 3-1. TYPICAL 52 I/O ASSEMBLY BEFORE TESTING

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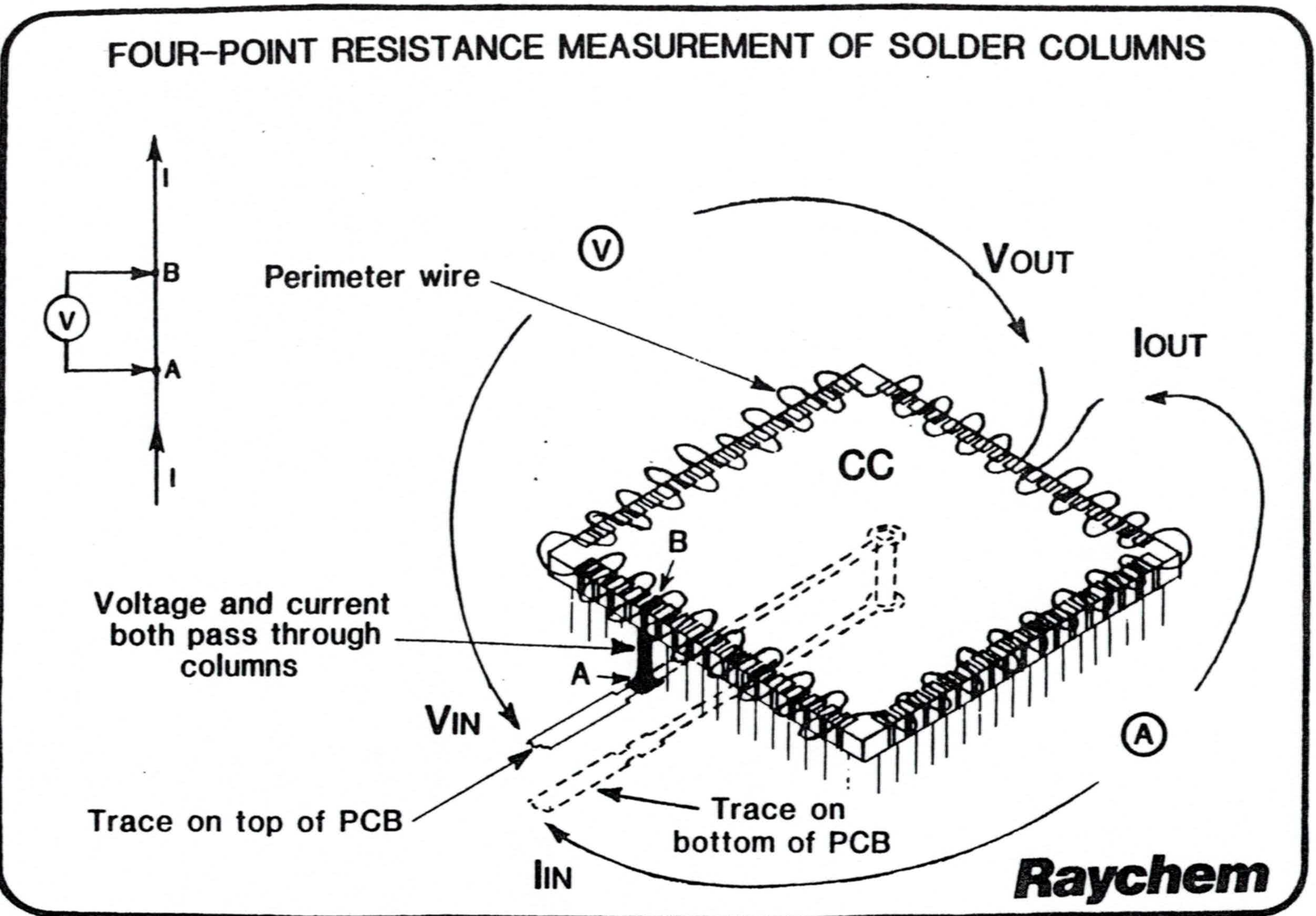
FIGURE 3-2



3.5 Tests

Two samples were subjected to temperature-cycle tests followed by shock tests followed by vibration tests. Electrical tests and visual inspection were performed between each test series. Resistance measurements were also made periodically within each test series.

3.5.1 Temperature-cycle: Samples were cycled between extremes of -55°C to +125°C with a 30-minute period, as shown in Figure C-1. Each sample was subjected to a total of 500 cycles.

3.5.2 Shock: Each sample was subjected to a series of shock tests at different G-levels. In each case, the sample received three shocks in each of six directions, for a total of eighteen shocks at each G-level.

300 G Pulse: Performed per MIL-STD-1344, Method 2004, Condition D (half-sine) for 3 millisecond duration.

1000 G Pulse: Performed per MIL-STD-202, Method 213, Condition E (half-sine) for 0.5 millisecond duration.

1500 G Pulse: Performed per MIL-STD-202, Method 213, Condition F (half-sine) for 0.5 millisecond duration.

3.5.3 Vibration: Each sample was subjected to 8 hours in each of two axes at 10.2 G RMS, per MIL-STD-1344, Method 2005.1, Condition VI (random).

Appropriate sections of the above military specifications are included in Appendix C.

3.6 Equipment

The test equipment used was calibrated with standards traceable to the National Bureau of Standards (NBS). A list of equipment appears below:

Temperature cycle:

Oven-Ransco Industries, Inc. Model 7304-3

Thermocouples-Omega Engineering, Inc., Chromel/alumel, copper/constantan

Cold junction compensation-Omega Engineering, Inc., Models MCJ-K and MCJ-T

Strip chart recorder-Cole-Parmer, Inc., Model R-8373-20 Dual channel

Digital multimeter-John Fluke Mfg. Co., Inc., Model 8840A, calibrated March 5, 1986.

Shock:

Shock machine, 300 G-Barry Controls, Inc., Model 15575, 15"X15" table, calibrated July 11, 1986.

Accelerometer- Endevco Corp., Model 2252, calibrated March 21, 1986.

Accelerometer amplifier- Endevco Corp., Model 2740B, calibrated March 17, 1986.

Oscilloscope- Tektronix Inc., Model 7633, calibrated March 18, 1986.

Oscilloscope sweep generator plug-in module- Tektronix Inc., Model 7B53A, calibrated March 18, 1986.

Oscilliscope time-base plug-in module-Tektronix Inc., Model 7A18, calibrated March 18, 1986.

Oscilliscope camera-Tektronix Inc., Model C-53

Shock machine, 1000, 1500 G- Avco Corp., Model SM105, 9-1/4" X 9-1/4" table, calibrated July 14, 1986.

Accelerometer- Endevco Corp., Model 2225, calibrated May 23, 1986.

Vibration:

Vibration system- MB Electronics Inc., Model C-60, rated 5000 force lbs, 5 Hz-3KHz, calibrated July 16,1986.

Accelerometer- Endevco Corp., Model 2275, calibrated January 31, 1986.

Accelerometer amplifier- Unholtz-Dickie Inc., Model D22-8, calibrated June 3, 1986.

Control system- Hewlett-Packard Inc., Model 5425A, calibrated June 17, 1986.

Sine/random signal vibration protector-Spectral-Dynamics Inc., Model SD123A, calibrated June 4, 1986.

Resistance measurements:

Datalogger-Acurex Corp, Model Autodata Ten/5

Power supply-Lambda Corp., Model LQ-520

Digital Multimeter-John Fluke Mfg. Co., Inc., Model 8012A

Digital Ohmmeter-Valhalla Instruments Inc., Model 4150ATC, calibrated November 7, 1985.

3.7 Conformance

Temperature-cycle tests were performed within Raychem and care was extended to ensure conformance to test specifications quoted in Paragraph 3.5. Thermocouples were used to monitor worst-case sample temperature and air-stream temperature in the test chamber. Traces of the thermocouple signals were recorded using a strip-chart for each of the 500 temperature cycles. The strip-chart recorder was periodically calibrated using NBS standard conversion charts and a 5-1/2 digit multimeter with accuracy traceable to NBS.

Shock and vibration tests were performed outside Raychem at Viking Laboratories, 440 Bernardo Avenue, Mountain View, CA. Raychem personnel were present and observed the tests at all phases. Certificates of conformance of the test procedures are included in Appendix C, along with copies of the data sheets corresponding to tests performed there.

Resistance measurements were performed using a four-probe technique which had an accuracy of +/- 1.0 milliohm. Values were recorded on an Acurex datalogger in conjunction with special circuitry constructed at Raychem which provided the current source for the four-probe technique. The resistance-measuring setup was kept in calibration in the following manner:

A pair of calibration cards were constructed with test circuit resistances representing high (37 milliohms) and low (6 milliohms) typical values. Circuit resistances on the cards were confirmed with a digital Ohmmeter which has calibration traceable to NBS. During operation of the resistance-measuring setup, the calibration cards were periodically scanned to confirm accuracy. Calibration card circuit resistance values taken periodically throughout the test program were recorded and are summarized in Figure C-2.

4.0 Results

4.1 Review of Previous Testing

Prior to the program described in this report, numerous independent tests were performed on different assemblies which were mounted using CCMD columns. Results of these tests give an indication of performance, but without the coupling of effects from combined testing. It should be noted that operating lifetime in a specific application will depend on a number of factors, including time-temperature history, package length dimension, column aspect ratio, PWB material and construction, and physical supports, such as heat sinks.

Tests were performed using JEDEC standard 68 I/O LCCC's with .050-inch pad spacing and glass-epoxy PWB's. Assemblies joined with .022-inch diameter, .100-inch high Soldercolumns survived a minimum of 1300 temperature cycles; assemblies made with .050-inch high columns of the same diameter surviveda minimum of 800 cycles. This may be compared to a performance of less than 50 cycles when assemblies with directly-mounted LCCC's were tested [5].

In independent mechanical tests, assemblies of 68 I/O LCCC's mounted with .022-inch diameter columns .100 inches high successfully survived 8 hours of random vibration in each of three axes at the 10.2 G RMS level per MIL-STD-1344, Method 2005.1, Condition VI. Similar assemblies survived three shocks in each of six directions at a 1000 G peak pulse level per MIL-STD-202F, Method 213B, Test Condition E.

A common behavior has been observed in the resistance of a column test circuit as temperature cycling progresses, as shown schematically in Figure 4-1. The curve shows a slow rise in column resistance over the majority of the temperature-cycle life. This rise corresponds to microcracks which develop in the body of the column and which tend to reduce stresses transmitted to the column end fillets.

At an advanced point in the cycle life, the column resistance begins to increase more rapidly. This corresponds to crack growth in column end fillets, primarily the fillet on the LCCC pad. Crack growth here may be attributed to the TCE mismatch between solder of the column end and the ceramic/metallization of the LCCC pad.

This effect produces a strain in the upper fillet which acts over the .022-inch diameter column end and which is reduced as the crack propagates, since the area over which the TCE

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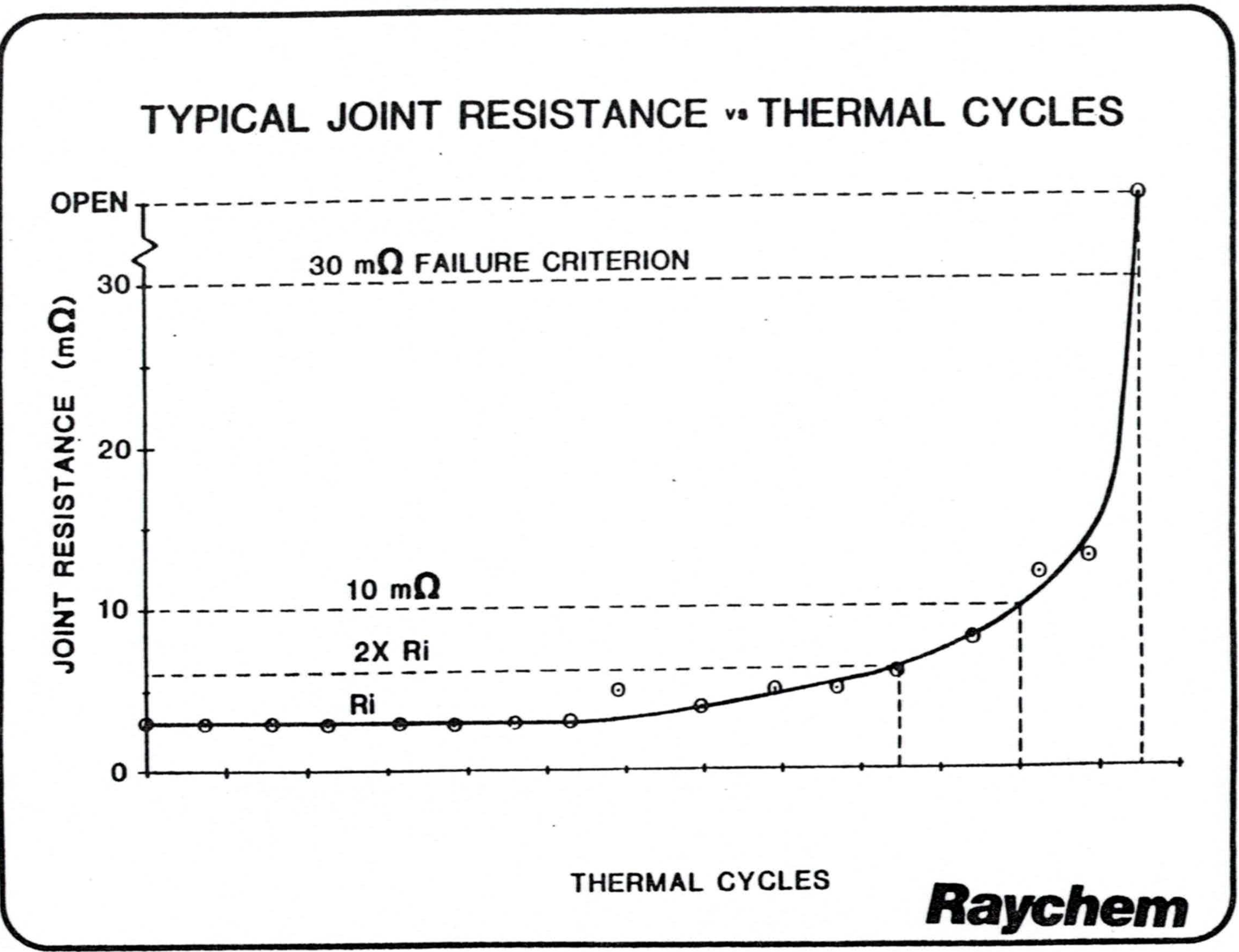
FIGURE 4-1



mismatch is effective becomes reduced. The end-fillet cracks in columns are therefore fundamentally different from those observed in directly-mounted solder connections, which are driven by a TCE mismatch between the ceramic package and the underlying organic PWB material.

Fillet cracks in Soldercolumns propagate more slowly than similar-looking cracks in solder joints of directly-mounted LCCC's for this reason. The result is a less drastic increase in column resistance with temperature-cycling, as shown in Figure 4-1, than the almost instantaneous electrical and mechanical failure observed with cracks in the direct-mount solder joints.

As cycling continues, column resistance rises more steeply. At the failure point, the resistance curve becomes vertical, indicating an open circuit. A value of 30 milliohms was chosen as the criterion which marks imminent electrical failure for this test program, as mentioned in paragraph 3.4.

4.2 Temperature cycle

In Figure 4-2 are shown typical thermocouple traces for the temperature-cycle tests. One (iron-constantan, or "type J") thermocouple (T/C) was attached to a sample PWB in the center of the test chamber. The other T/C (chromel-alumel, or "type K") was exposed to the moving air stream roughly in the center of the chamber.

In Figure 4-3 are shown column circuit resistance data for two typical 52 I/O assemblies from zero to 500 temperature cycles. The three curves represent the minimum, average and maximum test circuit resistances. The rise in resistance over the course of the temperature-cycle tests was less than 3 milliohms on average and less than 6 milliohms maximum.

In Figure 4-4 are shown circuit resistance values for the same two 52 I/O assemblies as a function of column location around the package periphery, before and after 500 temperature cycles.

In Figure 4-5 are shown photographs taken at 25X magnification of typical columns before and after 500 temperature cycles of testing. Small cracks are visible in the body of the columns at the interface between the reinforcing copper helix and the solder core. The beginnings of cracks also appear in some of the column upper fillets.

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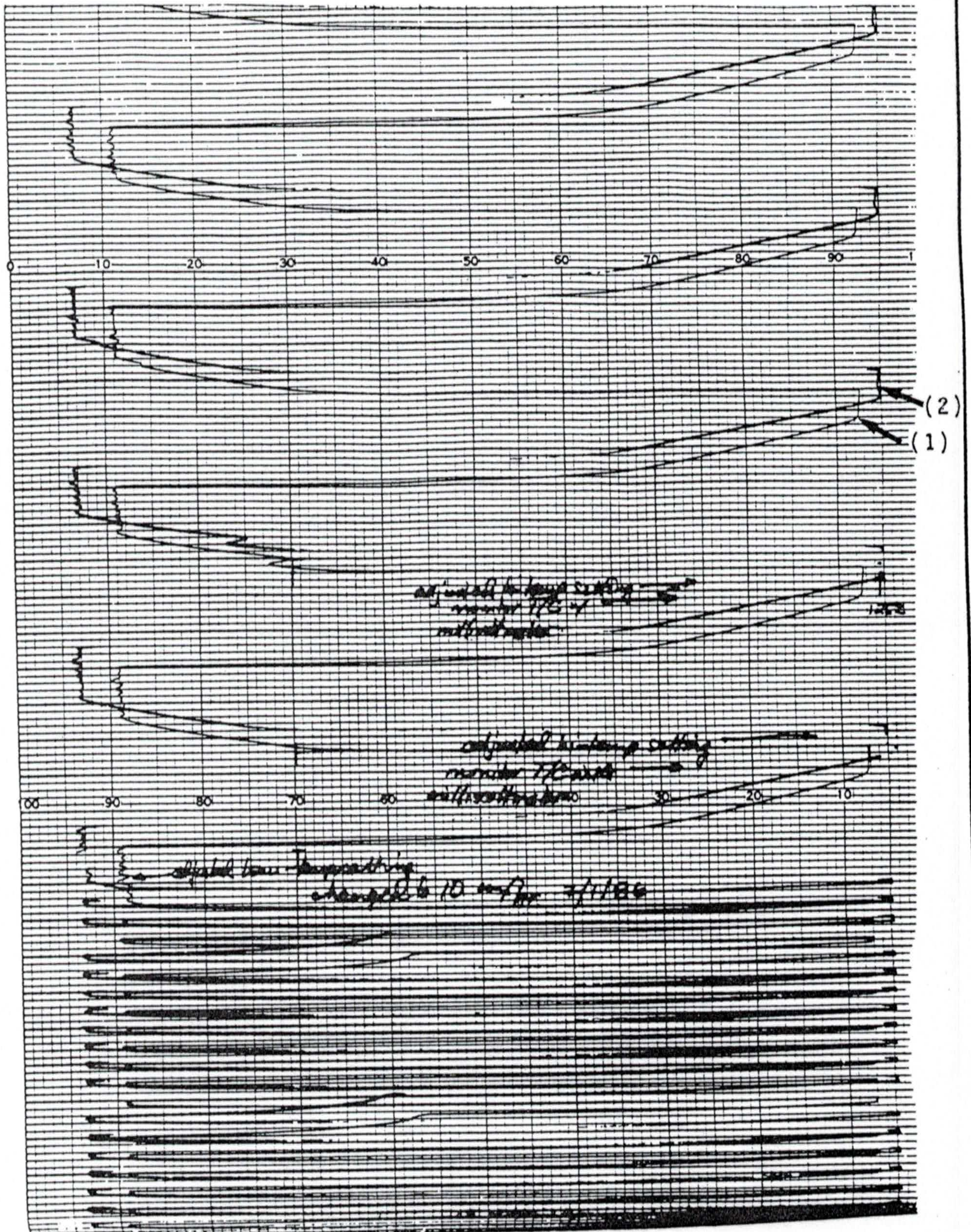

FIGURE 4-2. STRIP CHART TRACES OF THERMOCOUPLES IN AIR STREAM (1) AND IMBEDDED IN SAMPLE ASSEMBLY (2).

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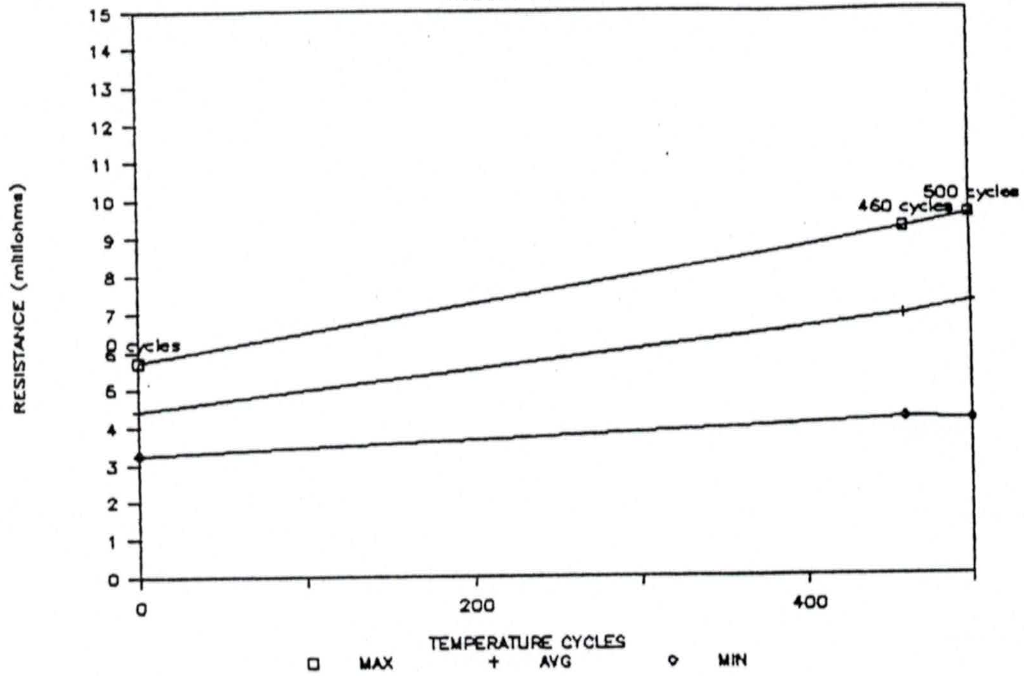

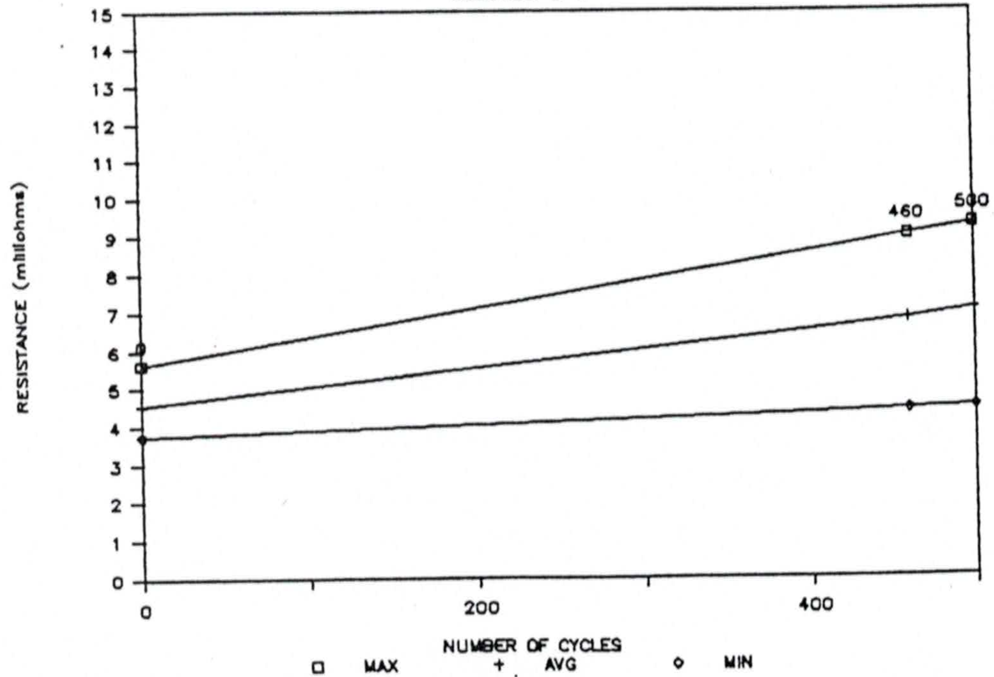

FIGURE 4-3. COLUMN RESISTANCE SUMMARY

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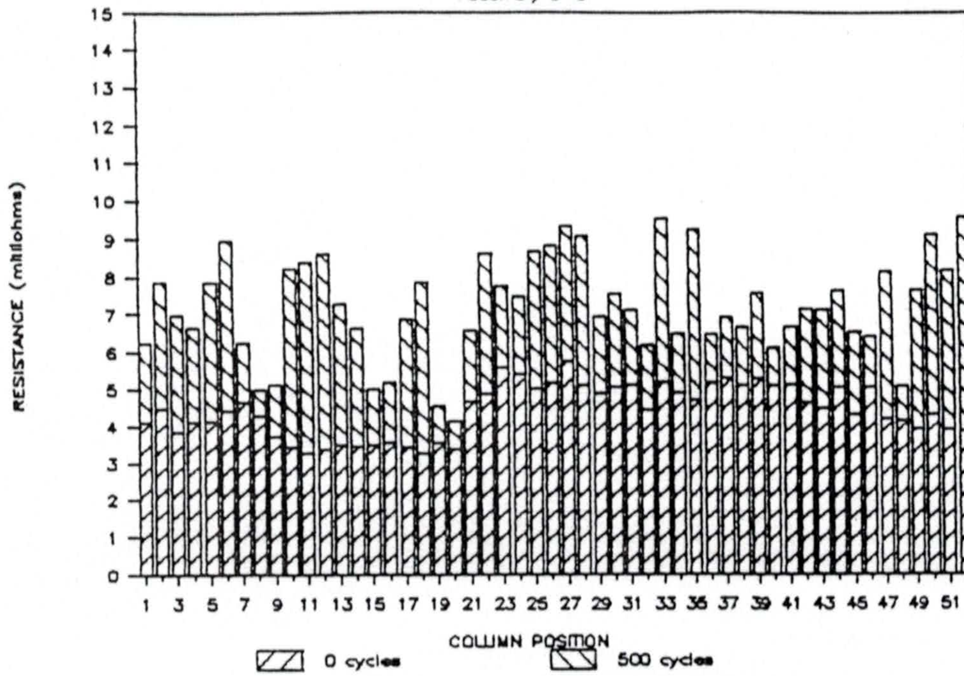


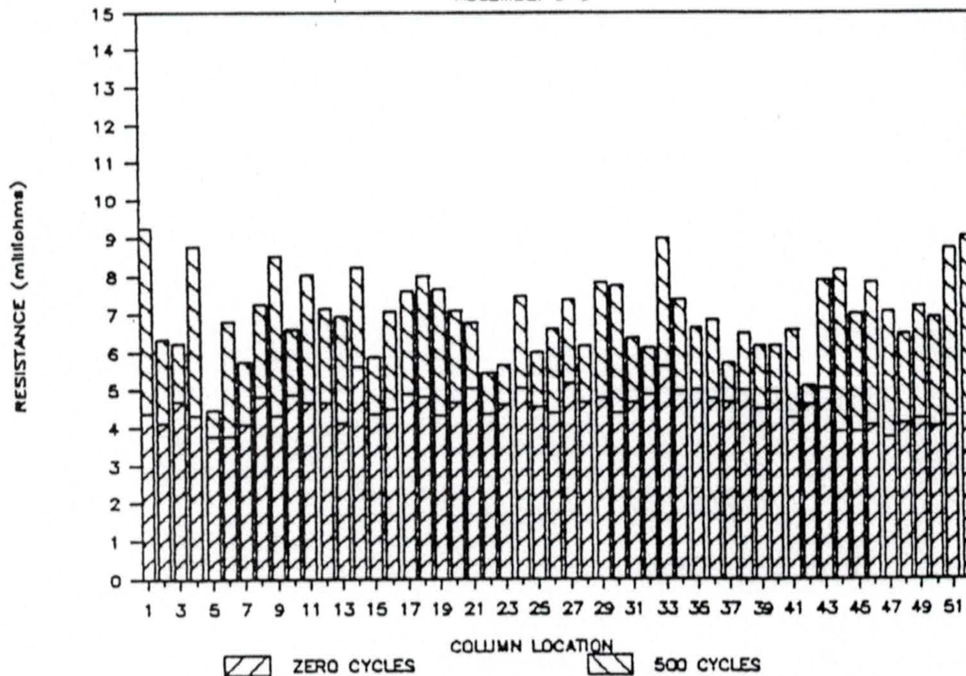
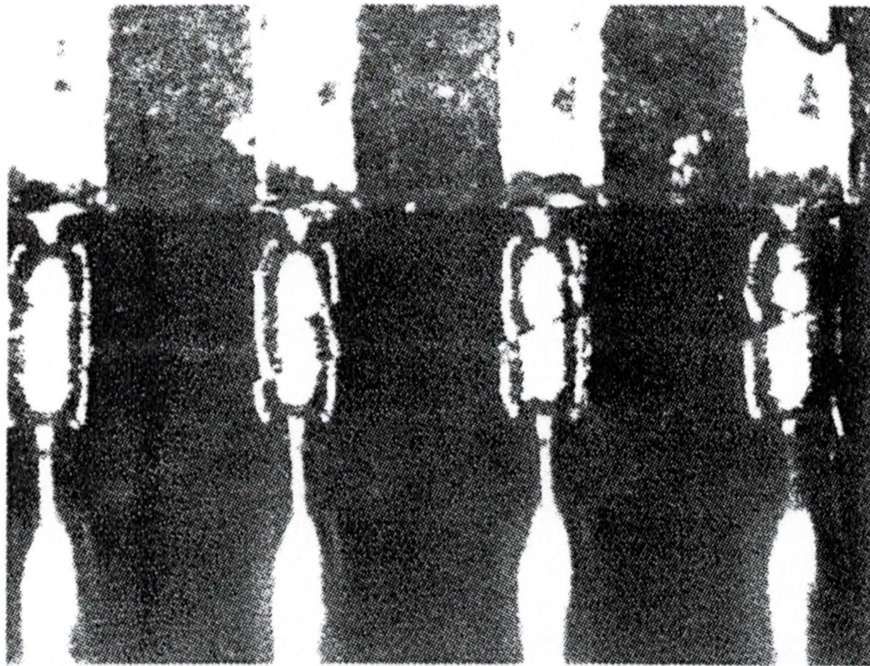
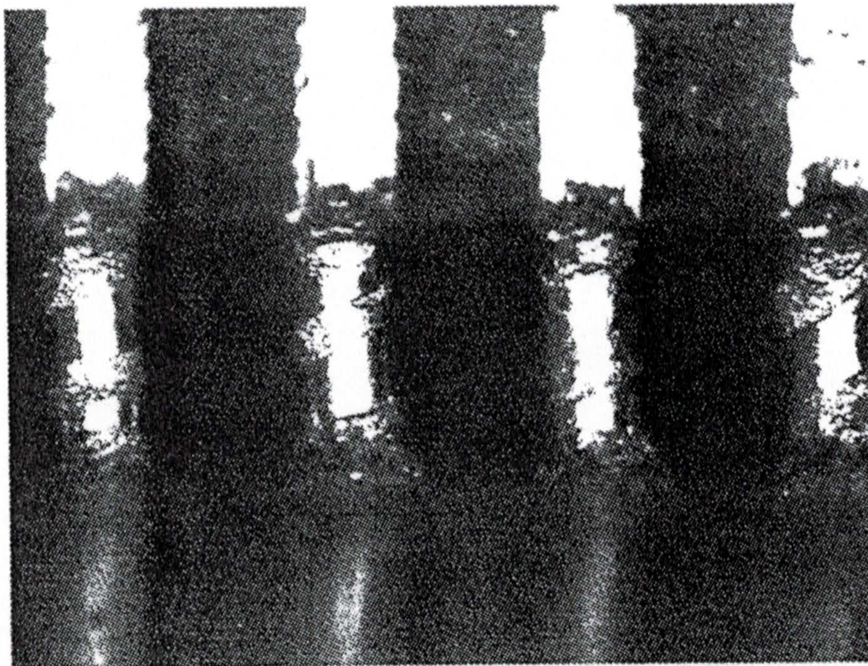


FIGURE 4-4. COLUMN RESISTANCE VS. LOCATION ON TWO ASSEMBLIES. LOCATION COUNT BEGINS ON LCCC PAD #1.



TYPICAL ASSEMBLY BEFORE TEMPERATURE CYCLING



ASSEMBLY 5-9 AFTER 500 TEMPERATURE CYCLES

FIGURE 4-5

4.3 Shock

Test assemblies were subjected to three (3) shocks in each of six (6) directions for a total of eighteen (18) shocks at each G-level. The G-levels tested were 300, 1000 and 1500 G peak, with durations of 3, 0.5 and 0.5 milliseconds, respectively.

Each sample was fixed to a mounting plate which was then bolted onto the shock table, as shown schematically in Figure 4-6. Samples were secured with four bolts through the PWB, one near each corner of the LCCC. An accelerometer was attached to the mounting plate near the PWB.

Typically, the shock table was raised to a pre-determined height and then dropped onto rubber mats which were chosen to provide the proper amount of damping. The accelerometer produced a signal proportional to its deceleration, which was thought to be representative of the shock experienced by the LCCC-column interconnection system.

Each of the shock pulses showed a half-sine acceleration characteristic with respect to time, as shown in Figure 4-7. This trace was taken on a 1500-G pulse with an accelerometer-amplifier sensitivity of 500 G/volt with no signal filtering.

In Figure 4-8 are shown resistance histories for two typical 52 I/O assemblies over the course of the entire shock test program. Measurements were made after each G-level shock series, beginning with 300 G and progressing to 1500 G shocks. Each assembly had experienced 500 temperature cycles prior to the shocks. The assemblies experienced a maximum resistance rise of no more than about 1.0 milliohm after completion of shock testing.

4.4 Vibration

Test assemblies were subjected to 8 hours in each of two primary axes; the Z- and either X- or Y- axis at a level of 10.2 G RMS, random. The test samples were secured to the vibration head using mounting plate fixtures as in the shock tests. An accelerometer was attached on the mounting plate which was vibrated in the Z-axis. The other sample was mounted so as to experience vibration in the X-axis. The frequency spectrum administered to the vibration head is shown in Figure 4-9.

In Figure 4-10 are shown plots of column resistance values of two representative assemblies over the course of the vibration program . Testing was performed in an alternating

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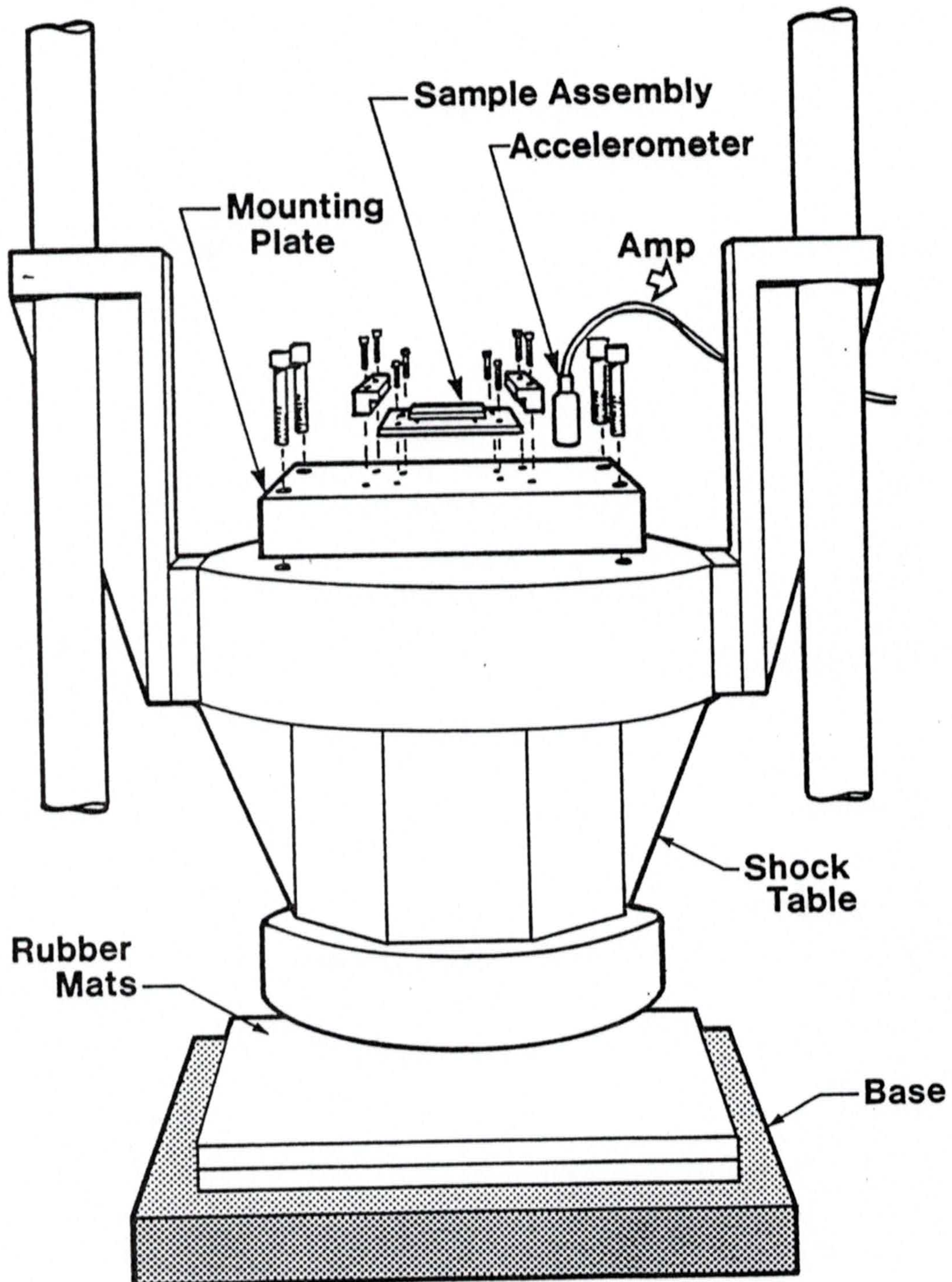

FIGURE 4-6. SCHEMATIC OF SAMPLE ASSEMBLY MOUNTED ON SHOCK TABLE.

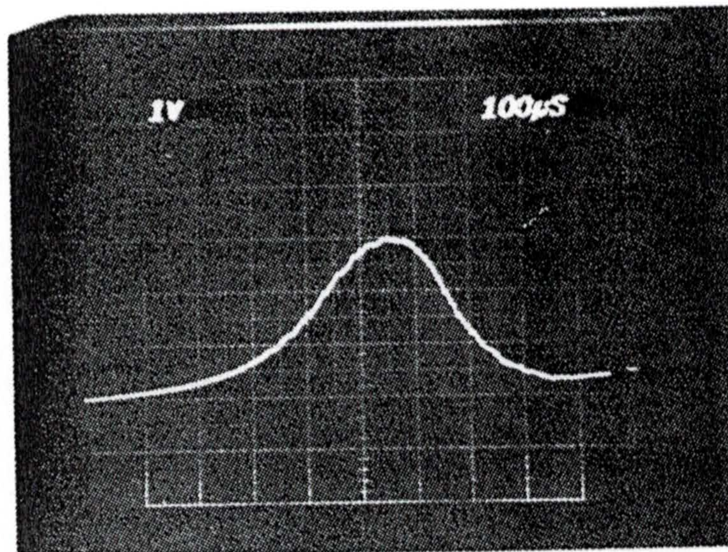

FIGURE 4-7. ACCELEROMETER SIGNAL TRACE
FROM 1500 G SHOCK TEST. SENSITIVITY IS 500G/V.

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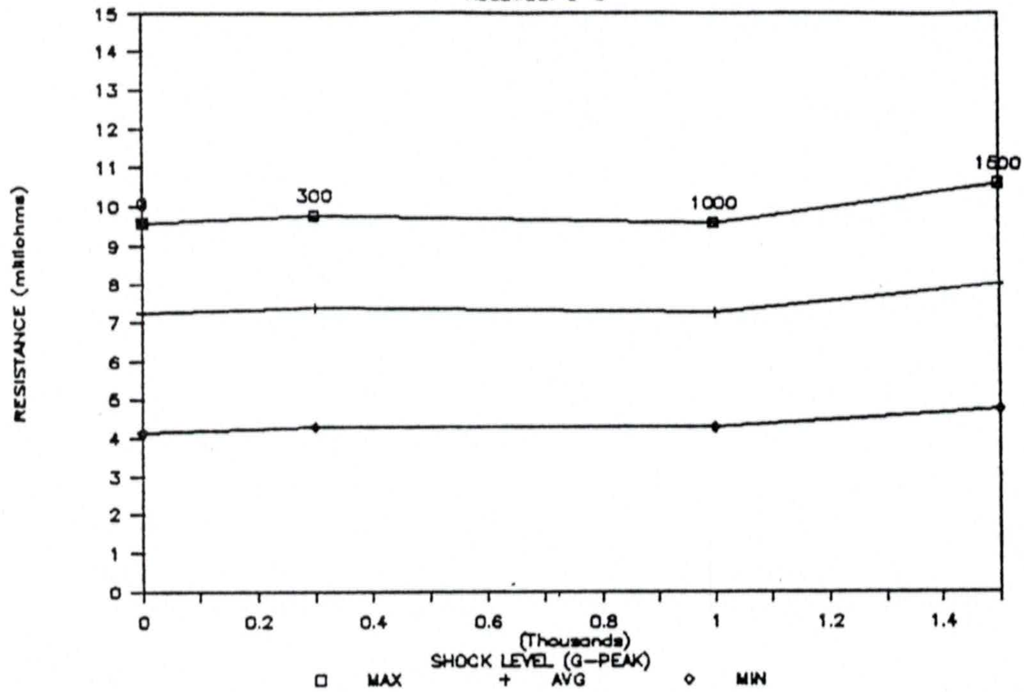

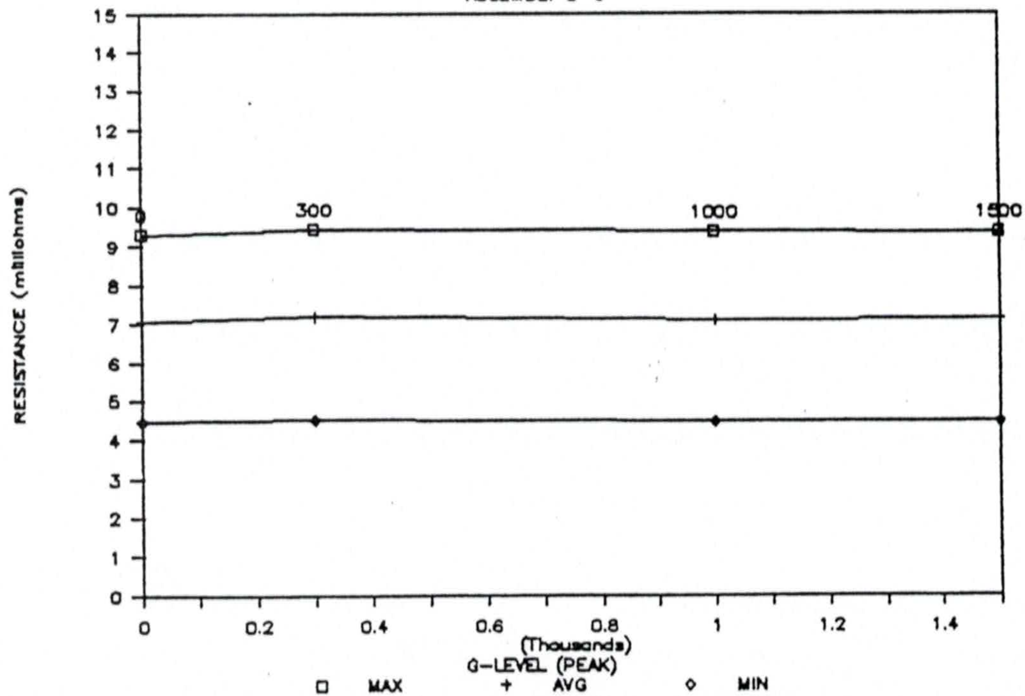

FIGURE 4-8. COLUMN RESISTANCE SUMMARY OVER SHOCK PROGRAM FOR TWO ASSEMBLIES.

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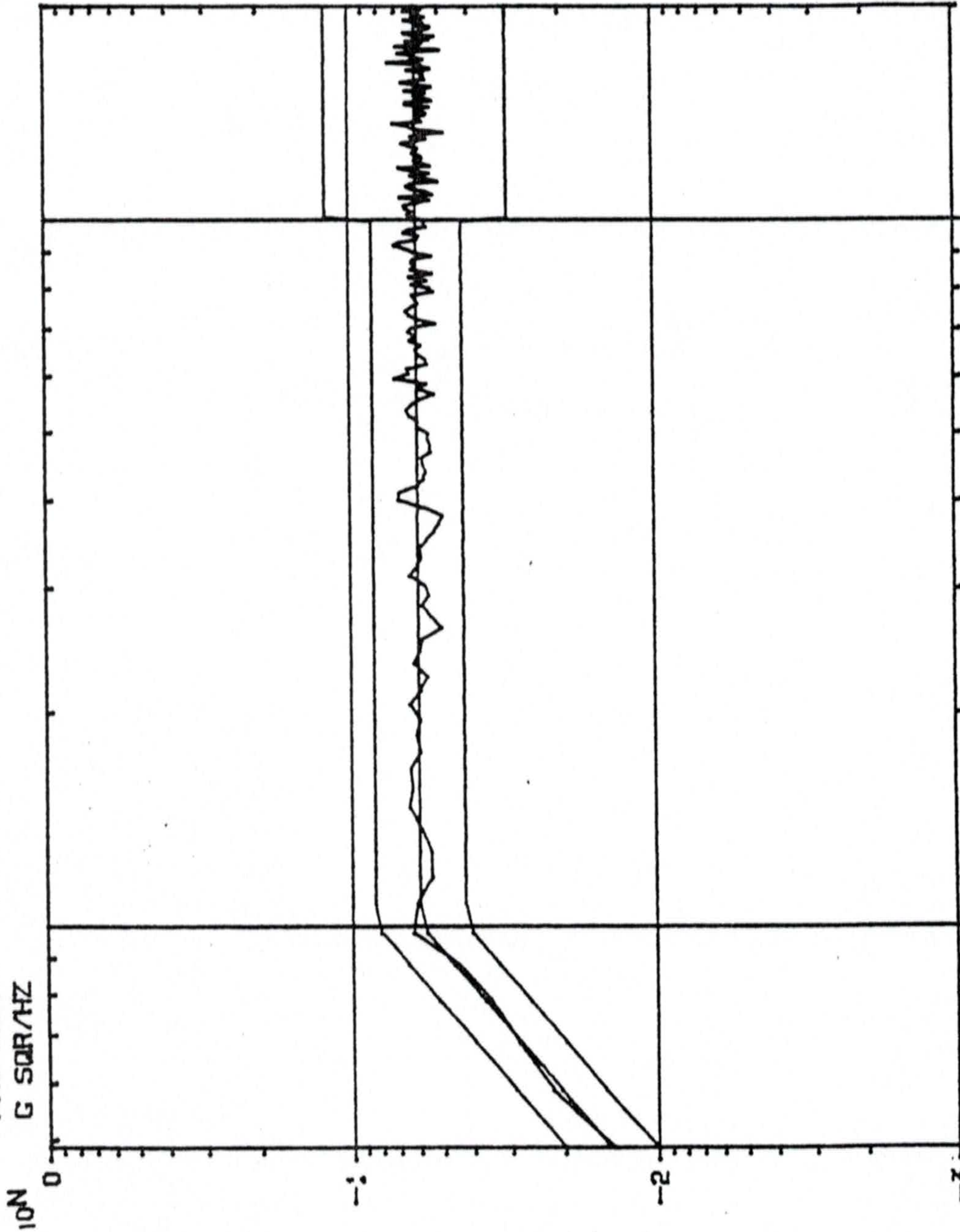

FIGURE 4-9. VIBRATION SPECTRUM ON MOUNTING PLATE DURING RANDOM VIBRATION TESTING.

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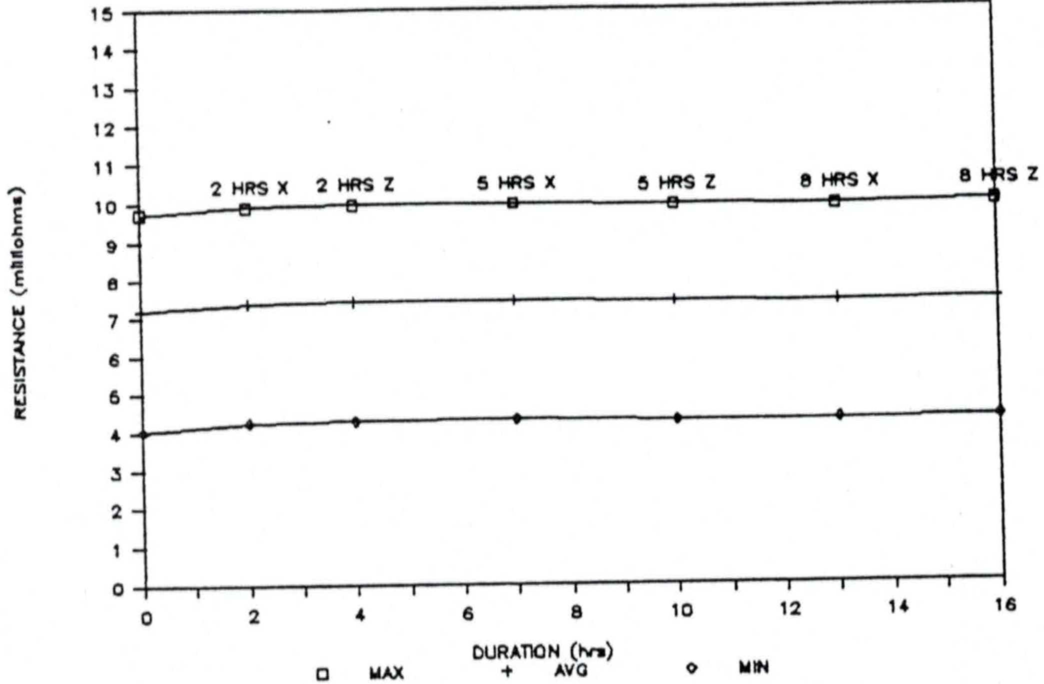


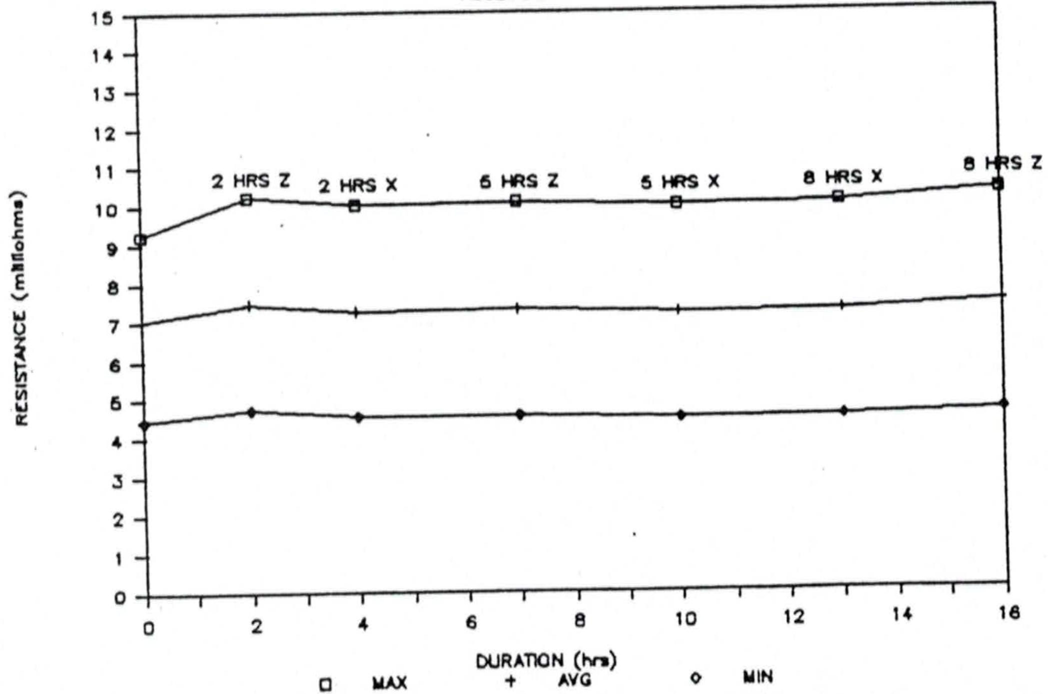
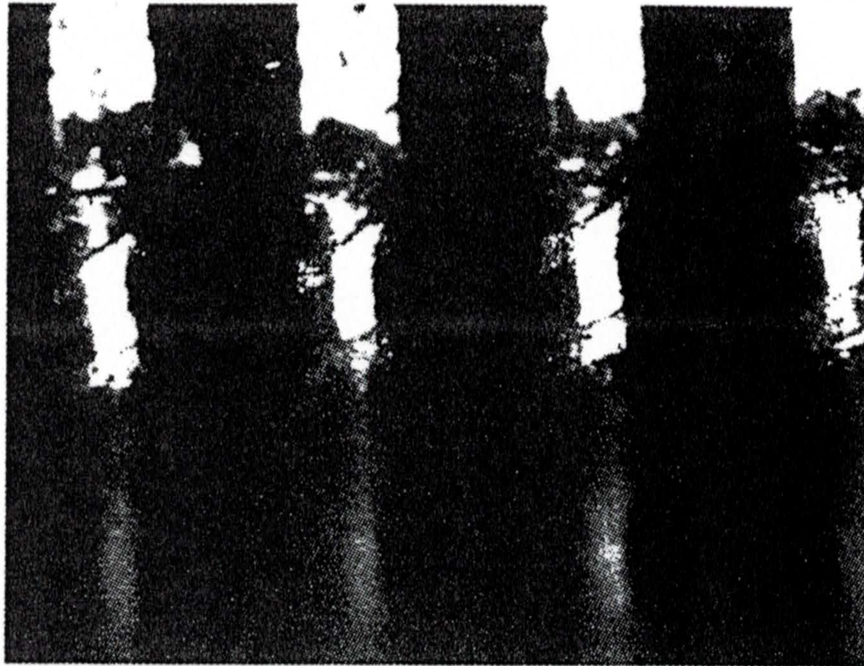


FIGURE 4-10. COLUMN RESISTANCE SUMMARY OVER VIBRATION PROGRAM FOR TWO ASSEMBLIES.

fashion, with each assembly accumulating a minimum of 2 hours in each axis before switching vibration direction. In the entire vibration testing program, the assemblies showed a maximum resistance increase of less than 1.1 milliohms.

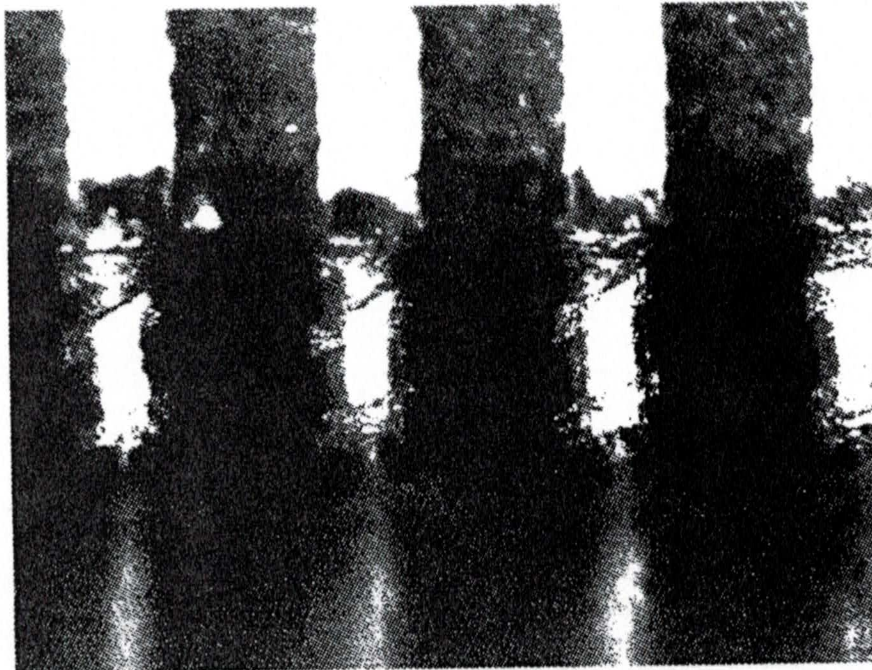
The maximum overall rise in resistance of any reading over the course of the test program was less than 7.2 milliohms. The maximum test circuit resistance was measured as 10.3 milliohms after testing was completed. Most of the resistance rise was associated with temperature-cycle testing, which accounted for a rise of less than 5 milliohms, maximum. Subsequent shock and vibration testing accounted for an increase of about 1 milliohm each.

In Figure 4-11 are shown photographs of the same columns which appear in Figure 4-5, after the entire thermal and mechanical test regimens had been run. At 25X magnification, cracks are visible in the bodies of the columns, as well as in the upper fillets.



5-9 NE Corner 25X 500 cycles

ASSEMBLY 5-9 AFTER 500 TEMPERATURE CYCLES



5-4 After shock + vibe NE Corner 11/5/86 25X

NE8

ASSEMBLY 5-9 AFTER COMPLETION OF TEST PROGRAM

FIGURE 4-11

5.0 Conclusions

Assemblies made with CCMD columns .022 inches in diameter and .050 inches high and with a JEDEC standard 52 I/O LCCC and glass-epoxy PWB's were shown to survive the combined thermal and mechanical testing program. Cracks in the body of the columns and in the end fillets were found not to have a detrimental effect on electrical and mechanical performance, causing a maximum resistance rise of 7.2 milliohms among the 104 circuits tested. The average resistance rise was about 3 milliohms. The resistance values measured before and after the test program were seen to be well below the 30 milliohm failure criterion in every case.

In applications where this combined test program is an appropriate measure of performance, the use of CCMD columns is judged to be suitable for the types of assemblies tested. Since the majority of resistance rise occurred in temperature cycling, assemblies which would experience less damage in temperature cycling could also be reasonably included in this conclusion. Such assemblies might have smaller LCCC outside dimensions, but would be identical to those used in this program in terms of package and substrate materials and column geometry. Included in this category would be the JEDEC standard LCCC's having .050-inch pad spacing and 52 or fewer leads, as well as the .040-inch spacing packages with 64 or fewer leads.

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