Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies With and Without Corner Staking

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***Abstract*—Area array packages (AAPs) with 1.27 mm pitch have been the packages of choice for commercial applications; they are now starting to be implemented for use in military and aerospace applications. Thermal cycling characteristics of plastic ball grid array (PBGA) and chip scale package assemblies, because of their wide usage for commercial applications, have been extensively reported on in literature. Thermal cycling represents the on-off environmental condition for most electronic products and therefore is a key factor that defines reliability.**

However, very limited data is available for thermal cycling behavior of ceramic packages commonly used for the aerospace applications. For high reliability applications, numerous AAPs are available with an identical design pattern both in ceramic and plastic packages. This paper compares assembly reliability of ceramic and plastic packages with the identical inputs/outputs (I/Os) and pattern. The ceramic package was in the form of ceramic column grid array (CCGA) with 560 I/Os peripheral array with the identical pad design as its plastic counterpart. The effects of the following key parameters on reliability of both CCGA and PBGA assemblies were investigated:

1) **thermal cycle ranges, −50 °C/75 °C, −55 °C/100 °C, and −55 °C/125 °C;**
2) **corner staking on failure mechanisms for two thermal cycle profiles, −55 °C/125 °C and −50 °C/75 °C;**
3) **package interchangeability, i.e., using PBGA package on CCGA pad design with a larger pad.**

Packages were assembled on polyimide boards and their daisy chains were continuously monitored. Optical photomicrographs were taken at various thermal cycle intervals to document damage progress and behavior. Representative samples along with their cross-sectional photomicrographs at higher magnification, taken by scanning electron microscopy and analyzed by energy dispersive X-ray, are also presented. The inspection documents were used to determine crack propagation and failure analyses for packages with and without corner staking. In assemblies with corner staking adhesive, a transition in failure from corner columns to center columns was observed when maximum temperature in thermal cycling profiles changed. This is a new failure mechanism not reported on in literature. Finite element analysis (FEA) was used to predict such global failure mode changes. FEA findings are also presented.

***Index Terms*—Ball grid array (BGA), ceramic column grid array (CCGA), column grid array (CGA), inspection, plastic ball grid array (PBGA), solder joint, stake, thermal cycle.**

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I. Introduction

BALL grid arrays (BGAs) and chip scale packages (CSPs) are now widely used for many electronic applications including portable and telecommunication products. 3–D/SiP development is the most recent response to further increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality. The BGA version has now started to be extensively implemented for high reliability applications with generally much harsher thermal and mechanical cycling requirements than those for commercial use. The plastic BGA (PBGA) version of the area array package (AAP), introduced in the late 1980 s and implemented with great caution in the early 1990 s was further evolved in the mid 1990 s to the CSP (also called fine pitch BGA, FPBGA) with a much finer pitch to 0.4 mm. Now, distinguishing between sizes and pitches has become difficult for the array packages.

These variety package styles with balls/columns underneath are now categorized as AAPs irrespective of the die/package ratios in order to be able to distinguish them from the flip-chip bare-die category. Bare dies have been around for a longer time, but their associated issues—including known good die and difficulty in direct attachment to printed wiring boards (PWB)—have limited their wide implementation. WLPs were introduced several years ago to address the key issues of bare die and to improve ease of handling and functional testing. As PWB technology with finer features becomes widely available with lower cost, use of bare die becomes more attractive.

Extensive work has been carried out by the JPL-led consortia in understanding technology implementation of AAPs for high reliability applications. This work (among other things) included assembly process optimization, reliability characterizations, and the use of inspection tools, including X-ray and optical microscopy for quality control and damage detection and calibration for as build and during environmental exposures. Lessons learned by the team have been continuously published [1]–[5].

This paper will first provide a summary of most recent assembly reliability data presented on in literature for inputs/outputs (I/Os) from 255 to 1657 and pitches to 1 mm for ceramic ball grid arrays (CBGAs) and ceramic column grid arrays (CCGAs). Then, it will provide details on design and assembly of the experimental test vehicles including the design of PWB and solder paste print efficiency using automatic and manual printing. Manual printing using mini-stencil was needed in order to have much higher localized solder paste

TABLE I
CYCLES-TO-FAILURE DATA ILLUSTRATING THE EFFECT OF A NUMBER OF KEY VARIABLES)

Case Number	Package-I/O, Pitch	Pkg Size (die size) mm	Thermal Cycle Condition (ramp, dwell, Cycle/hr)	First Failure	Mean Life ($N_{63.2\%}$)	Comments
1	CBGA-255-1.27	21x21 (1mm substrate)	0° to 100°C (10, 5, 2cycles/hr)	1,980 (1% failure)	2,426 ($N_{50\%}$)	PWB, 1.55mm thick (Thk) Ref. [14]
2	CBGA-361-1.27	25x25 (substrate 0.8 mm Thk)	0° to 100°C (3 cycles/hr)	NA	4,535 ($N_{50\%}$)	Avg solder paste vol 5,900 mil^3 PWB, 1.57 mm Thk Die 15x10 mm[14]
3	CBGA-361-1.27	25x25 (substrate 1.2 mm Thk)	0° to 100°C (3 cycles/hr)	NA	2,700 ($N_{50\%}$)	Note: Increase from die Thk .8 to 1.2 and 2.9, reliability reduction by 1.8 and 3.2 times Ref [9]
5	CBGA-625-1.27	32.5x32.5 (substrate 0.8mm Thk)	0° to 100°C (3 cycles/hr)	NA	2,462 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref [10]
6	CBGA-361-1.27	25x25 (substrate 0.8 mm Thk)	–55° to 110°C (2 cycles/hr)	890 (100 ppm)	1,190 ($N_{50\%}$)	PWB, 1.57 mm Thk Ref [10]
7	CBGA-361-1.27-HiCTE Substrate	25x25 (substrate 0.8 mm Thk)	–55° to 110°C (2 cycles/hr)	1,310 (100 ppm)	2,160 ($N_{50\%}$)	Substrate CTE, 12.2 ppm Ref [11]
8	CGA-361-1.27-Interposer	25x25 (substrate 0.8 mm Thk)	–55° to 110°C (2 cycles/hr)	1,350 (100 ppm)	2,320 ($N_{50\%}$))	NTK Interposer CGA PWB, 1.57 Ref [10]
9	CGA-361-1.27-IBM	25x25 (substrate 0.8 mm Thk)	–55° to 110°C (2 cycles/hr)	1,080 (100 ppm)	1,520 ($N_{50\%}$)	Ref [10]
10	CBGA-1681-1.27-HiTCE	42.5x42.5x1.85 substrate)	–25° to 125°C (1, 9min, 3 cycles/hr)	613 (1^{st} failure)	1,142 ($N_{50\%}$)	PWB, 93 mm Thk Ref [11]
11	CBGA-625-1.0	32x32x2.4mm (substrate)	0° to 100°C (2 cycles/hr)	NA	740 ($N_{50\%}$)	Ref [12] IBM-2003
12	CBGA937-1.0	32x32x1.5 (substrate) 32x32x2.4	0° to 100°C (2 cycles/hr)	NA	1,860 ($N_{50\%}$) 1,310 ($N_{50\%}$)	Refe [13]
13	CCGA1657-1.0	42x42x1.5 42x42x2.55 42x42x3.7	0° to 100°C (2 cycles/hr)	NA	1,530 ($N_{50\%}$) 990 ($N_{50\%}$) 620 ($N_{50\%}$)	Ref [12]
14	CCGA 1657-1.0 Cu	42.5x42.5x 2.55	0° to 100°C (2 cycles/hr)	1,660 (1^{st} failure)	2,410 ($N_{50\%}$)	Cu Column, solder paste 96.5 Sn3.5Ag Ref [13]

print recommended for CCGA package assembly. The test vehicles (TVs) were subjected to profiles. The thermal-cycle data and cross-sectional photomicrographs for the TVs including both CCGAs and PBGAs under three different thermal-cycle regimes with and without corner staking adhesives are also presented. The new failure mechanisms detected for CCGA

assemblies due to maximum temperature exposure and corner staking are discussed in details. Finally, finite element analysis (FEA) simulation analysis results for the two cases are summarized.

II. Literature Review on Second-Level CCGA Reliability

Area arrays come in many different package styles. These include plastic ball grid array with ball composition of eutectic Sn63Pb37 alloy or its slight variation. The ceramic BGA package uses a higher melting ball (Pb90Sn10) with eutectic attachment to the die and board. The column grid array (CGA or CCGA) is similar to the BGA except that it uses column interconnects instead of balls. The lead-free CCGA uses copper instead of high melting lead/tin column. The flip chip BGA (FCBGA) is similar to the BGA, except that the flip chip is internal to the package and a flip chip die is used.

Three BGA package configurations are popular. These are: a) full array; b) staggered array; and c) peripheral array. Plastic packages come in all styles whereas ceramic package are generally limited to the full array configuration. Fully populated array packages presents some significant routing challenges if conventional PWB with plated through-hole (PTH) vias are considered for the design. Peripheral plastic packages have been developed to reduce solder joint failures at the die edge as well as to improve routability characteristics. However, for ceramic package there is a lesser need for peripheral array because the CTE mismatch between the die and package material is negligible.

Most ceramic packages are supplied in full array configuration. The CCGA used in this investigation; however, was a peripheral array possibly because the package was designed such that pad pattern simulates its plastic package version.

Table I lists cycles to failure for a number of CCGAs/CBGAs with different configurations, selected from the very limited data set reported in the literature [9]–[13]. Data were chosen to be able illustrate the effects of a few key parameters on reliability. The following parameters were considered when test data were tabulated even though in some cases specific information was not reported and in fact was missing [14].

A. Thermal Cycle Range, Ramp Rate, Dwell Times

For example, the cycles-to-fifty percent-failure (CT50%F) for the CBGA 361 I/Os over the range of 0 °C/100 °C was 4535 cycles (Case #2); it reduced to 1190 cycles when the temperature range broadened to −5555 °C/110 °C (Case #6).

B. Package Size, Thickness, Materials, Configuration, And I/Os

Comparing Case #2 to Case #3, a relatively large reduction in CT50%F is shown when the package thickness is increased from 0.8 mm to 1.2 mm (4 535 versus 2700 cycles). When the package thickness is further increased to 2.9 mm, the CT50%F is further reduced, a reduction by 3.2 times relative to the package with 0.8 mm thickness. A similar reduction was observed for the CCGA 1657 I/Os when the package thickness is increased from 1.5 mm to 3.7 mm (Case #13). The reliability decreases by increasing the package I/O since the distance to the neutral point is increased. CT50%F is reduced from 4535 cycles to 2462 cycles when the I/Os for the 0.8 mm thick package is increased from 361 to 625 (Case #2 versus Case #5). Use of higher CTE ceramic materials—to better match the ceramic CTE to the PWB—will also improve the reliability. For example, compare Case #6 to the Case #7 for the 361 I/O CBGA assemblies. The CT50%F increased from 1190 to 2160 cycles for the high coefficient of thermal expansion (HiCTE) package.

C. Die Size and Its Relation to the Package Size and Ball Configuration

The effects of die size and package configuration (full versus peripheral) arrays on reliability are more pronounced for plastic rather than for ceramic package assemblies.

D. PWB Thickness, Definition of Pad, Surface Finish

The preferred thickness was defined as 2.3 mm in IPC-9701A [6] since it is known that generally plastic packages assembled on thinner PWBs show higher cycles-to-failure. The effect of board thickness for ceramic packages is not yet well established, but its effect may be less critical for the column grid array than for plastic package assemblies, especially when the dominant failure is the columns rather than solder joints.

E. Single Side or Double Side, Relative Offset of Package on Top and Bottom

This is not shown here, but discussed by this author in other papers [7], [8]. Reliability decreased for double-sided mirror-imaged or partially offset PBGA assemblies. The effect of mirror image assemblies on reliability for CBGAs/CCGAs is not presently known.

III. Effect of Solder Joint Volume on CCGA Assembly Reliability

In contrast to PBGA assemblies, CCGAs/CBGAs assembly reliability is significantly affected by the amount of solder volume. In fact, solder volume is the most important key process variable affecting the reliability of CCGA/CBGA assemblies. Recommended minimum, optimum and maximum solder paste volumes for both CBGA and CCGAs are shown in Table II [15], [16]. The effect of solder volume for CBGAs is intuitive since higher solder volume increases the solder balls' stand-off height, but this is not the case for the CCGA assemblies where column flexibility also plays a role in reliability.

For CBGAs, it has been shown that increasing solder-paste volume increases reliability, but only up to a point. When the paste volume passes 10 000 cubic mils (0.16 cubic mm), the reliability no longer increases because the solder paste has filled the area between the ball and the card. Additional solder paste moves up the ball toward the module, making the ball look like a column. When the fillet dimension at the card surface is maximized, so is the reliability.

This trend may not be true for at least one type of CCGA package, the one with 1.27 mm pitch. Unlike the CBGA product, high solder paste volume can actually start to decrease the interconnection reliability. As the volume increases, so does the fillet height on the column. This increased fillet height

TABLE II
SOLDER PASTE RECOMMENDATION FOR CBGA AND CCGA, 1.27 MM PITCH

Component Type	Minimum Paste Volume mil^3 (mm^3)	Optimal Paste Volume mil^3 (mm^3)	Maximum Paste Volume mil^3 (mm^3)
CBGA	4800 (0.089)	6500-7500 (0.10-0.20)	10000 (0.160)
CCGA	3000 (0.0470)	5000-5600 (0.078-0.088)	7600 (0.120)

reduces the effective length of the flexible column, thus making it stiffer. This effect—while true for both cast and wire—is more pronounced for the cast because it is stiffer in nature due to its larger diameter [16].

In a comprehensive investigation performed for this category of packages, it has been shown that assemblies with a minimum acceptable solder paste showed slightly higher reliability than those with nominal and much better than those with higher solder volume. To avoid inducing opens however, the use of nominal rather than minimum solder paste volume is recommended.

IV. OBJECTIVES

The purpose of this investigation was to characterize the reliability of AAPs with the 560 I/Os. This included ceramic column grid array and its plastic counterparts with the identical peripheral package configuration. A designed experiment was utilized to cover many aspects that are considered to be unique for the potential use of these packages. Solder joint reliability is affected by many variables as briefly discussed in the previous section. The following parameters were either characterized or evaluated as part of the DOE implementation.

1) Two pad designs, one for the CCGA and smaller pads for PBGA attachment. PBGAs were assembled on both pad sizes to evaluate PBGA interchangeability with the CCGA.
2) Two stencil designs, a relatively thicker mini-stencil especially designed for CCGAs and a standard stencil to assemble PBGAs and other surface mount packages. Solder paste print volumes further varied by changing the stencil thickness and opening. Measured solder paste print volumes for a few samples area shown in graphs.
3) Vapor phase reflow for tin-lead solder with constant reflow temperature of 217 °C for 60 s were used to assemble CCGA and PBGAs.
4) CCGA and PBGA assemblies without and with corner stake adhesive bonds. Corner stakes were added after solder joint assembly. Corner adhesive bonds are used to improve resistance to mechanical vibration and shock loads.

The assemblies were subjected to three types of thermal cycles. Both the process and reliability results for CCGA package assemblies are discussed and compared to their PBGA counterparts.

V. TEST VEHICLES

Polyimide printed wiring boards (PWBs) were designed to accommodate two pads configurations, one for the PBGAs and the other for the CCGAs. Polyimide rather FR-4 PWB is commonly used for high reliability applications. The pad sizes for the PBGA and CCGA were 24 and 33 mils, respectively. The traces from the pads were attached to plated-through-hole, (PTH) vias with 24 mil diameters. Specific pairs of pads were connected through PTHs and these connections within a package pair completed daisy chain patterns to be used for solder joint continuity monitoring. Four key daisy chains for each package were used for continuous monitoring during thermal cycling. Four additional pads were added at each side of the package for manual probing and failure identification. The probing pads were used when an overall failure is detected through continuous monitoring.

Similarly, two daisy chain sets—each with three rows, using PTH vias representative of the test design—were added to monitor the behavior of the PTHs during thermal cycling. Continuity of the PTH daisy chains was performed manually at each thermal cycle interval when the assemblies were removed from the chamber for inspection. The PWB's pads had hot air solder level (HASL) surface finish. HASL and organic solderability preservative (OSP) surface finishes are specified in IPC-9701A as the recommended surface finishes for tin-lead solder attachment reliability evaluation. The key reason for such recommendation is to avoid potential premature intermetallic failures such as those occasionally observed for the ENIG (electroless nickel/immersion gold) surface finish. Because of space availability, additional parts such as leaded and leadless packages and capacitors were added in order to assess their reliability; reliability of these conventional packages is not discussed in the paper. Fig. 1 shows the top and bottom of the board design showing the daisy chain configurations for the packages, probing pads, and PTH vias.

VI. STENCIL DESIGN, PASTE PRINT, AND VOLUME MEASUREMENT

In a previous study, only the 8 mil (200 μm) thick stencil thickness was used to assemble both CCGA and surface mount components. However, to achieve optimum solder paste volume for CCGA and SM assemblies, two stencil types with two different thicknesses were used. Much higher solder volume was recommended to be used for CCGAs by the package supplier. Table III lists estimated solder paste volumes that can be achieved with different stencil thicknesses and aperture openings. The 7 mil stencil thickness represents the general stencil that could be used for paste application on PBGA and other package pad patterns. The mini stencil with 10.5 mil thickness was used only for the manual paste print application for CCGA in order to achieve the higher paste volume recommended by the package supplier. Previously, it was shown that a higher

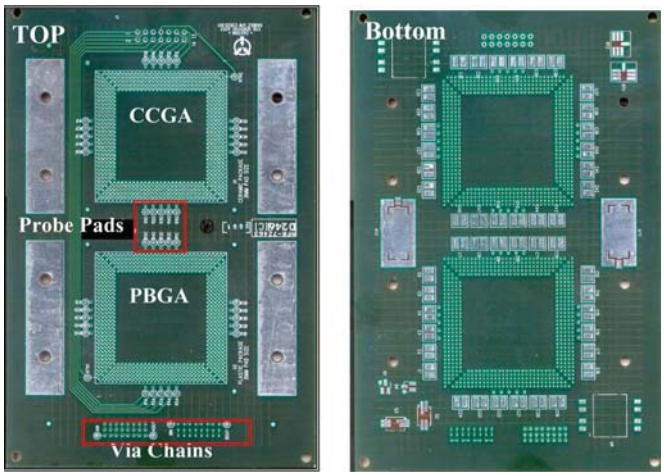

Fig. 1. Printed wiring board design showing package daisy chain, probing pads, and via daisy chains.

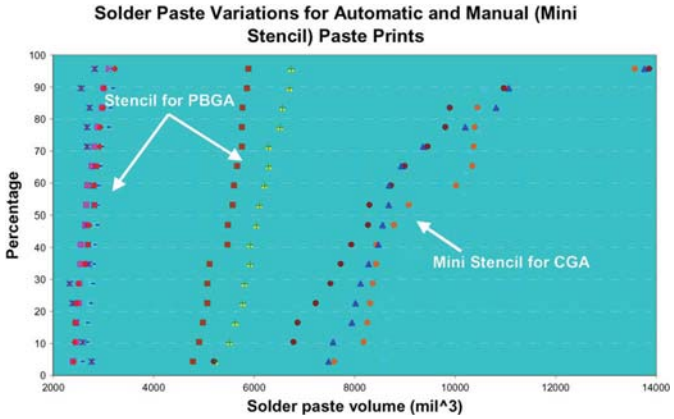

Fig. 2. Paste volume variations and the effect of automatic and manual using mini-stencil for printing.

TABLE III
STENCIL PARAMETER AND SOLDER VOLUME

Stencil Thickness	Solder volume $(mil)^3$	Option
BGA-Aperture 23 mil-Stencil 7mil	2909	Stencil
BGA-Aperture 24 mil-Stencil 7 mil	3168	No
CCGA-Aperture 32 mil dia-stencil 7 mil	5632	Stencil
CGA-Aperture 33 mil dia-stencil 7 mil	5990	No
CCGA- Aperture 32 mil dia- Stencil 8 mil	6430	Stencil (Previous study)
CCGA-Aperture 32 mil dia-stencil 10.5 mil	8440	Mini-stencil

solder paste volume could improve the reliability of CBGAs and CCGAs with 1.27 mm pitches. The effect of higher solder volume in improving solder joint reliability is now being questioned for the CCGAs (see Table II).

An RMA paste, type III ($-325+500$) mesh paste was used for paste printing using automatic and normal manufacturing parameter setup for the case of the 7 mil stencil thickness. Manual paste printing was performed when the mini-stencil was used. After printing, each paste print on the PWB was visually inspected for gross defects such as bridging or insufficient paste. Paste print quality was improved by adding paste when insufficient paste was detected and solder paste was removed when bridging condition discovered. Solder paste heights were measured using a laser profilometer. Measurements were made at numerous locations including corner and peripheral pads to gather solder volume data and their corresponding distributions.

Fig. 2 shows plots of solder volume distribution for two different stencil thicknesses (7 and 10.5 mil) and pad opening for the 7 mil stencil thickness. Note the solder paste height measurement was done relative to the PWB surface rather than the Cu (copper) pad; therefore, the heights are a Cu thickness higher than their actual values. No adjustments were made when the solder volume was calculated based on the height and the pad diameter. It is apparent that mini-stencil produced a wider distribution in the solder paste volume than that can be achieved through automatic printing. Improvement in the distribution was improved slightly after a second manual printing, but the distributions are still much wider than in the automatic version.

VII. DESIGNED EXPERIMENT FOR ASSEMBLY

The objectives and parameters considered in the designed experiment were discussed previously. Packages are 42.5 by 42.5 mm in dimension; they are peripheral array with five rows and 1.27 mm pitch. The CCGA has a 0.2 mm ceramic interposer between the package and the column and a gap of 0.1 mm between the interposer and the package. The solder column is a high melt solder with a diameter of 0.89 mm and a height of 1.62 mm. The plastic package had a cavity down configuration with the die directly attached to an integrated copper heat sink. Solder balls were tin/lead eutectic with 0.75 mm in diameters.

VIII. INSPECTION BEFORE ENVIRONMENTAL TESTS

For high reliability electronic applications, visual inspection is traditionally performed by Quality Assurance personnel at various levels of the packaging and assembly, known as mandatory inspection points (MIPs). Solder joints are inspected and accepted or rejected based on specific sets of requirements. Further assurance is gained by subsequent short-time environmental exposure, by thermal cycling, vibration, and mechanical shock, and so forth. These screening tests also allow detection of anomalies due to workmanship defects or design flaws at the system level. For space application, generally 100% visual inspection is performed at prepackage prior to its closure (precap) and after assembly prior to shipment.

Visual inspection is only somewhat useful for the AAPs since obviously it is of no value for hidden balls and columns under the package. X-ray inspection is needed for AAPs. However, in the case of CCGAs, the hidden solder joint could not be distinguished because of the heavy ceramic lid that inhibited X-ray penetration [7]. Visual inspection can often be used in examining CBGA and CCGA assemblies since generally the solder

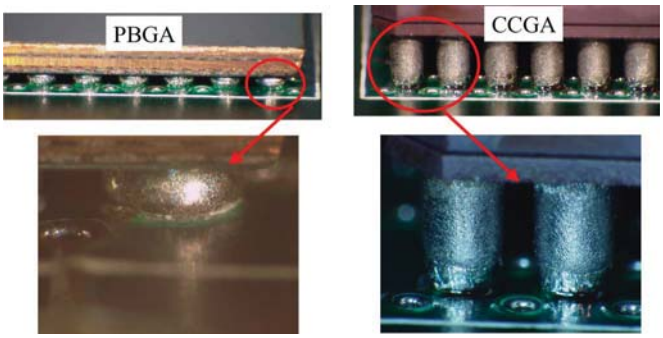

Fig. 3. Optical photomicrographs of PBGA and CCGA after assembly.

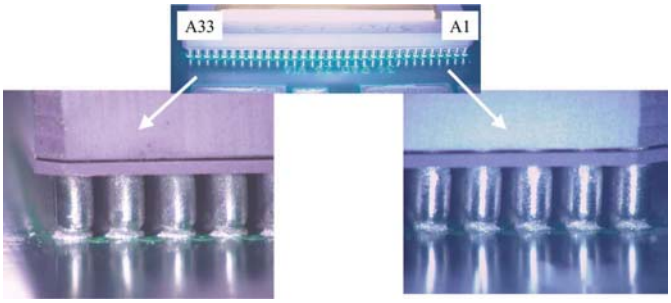

Fig. 4. Optical photomicrographs of CCGA built with 8 mil thick stencil after 200 cycles (−55 °C/100 °C). Note graininess and solder loss as well as solder column shifts at corners.

fails at the exposed corners or periphery ball attachments. Peripheral balls and columns were inspected visually using an optical microscope at the start and during thermal cycling to document damage progress. Fig. 3 shows photomicrographs of solder joints of PBGA and CCGA assemblies prior to thermal cycling.

IX. Thermal Cycle Test

An industry-wide guideline document, IPC SM-785, for accelerated reliability testing of solder attachment has been in existence for more than two decades. Only recently, industry has agreed to release an industry-wide specification, IPC-9701, in response to BGA and CSP technology implementation [6]; its revision A now includes a guideline for Pb-free solder evaluation. Although very valuable and still valid, the IPC SM-785 guideline did not answer the key question of what the data means in terms of product application and data comparison. As is well established by industry and the JPL Consortia [1]–[5], many variables could be manipulated to either favor or disfavor test results.

Also, in some cases, considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing intermetallic rather than solder joint failure. This mishap is especially likely to occur by a novice user/supplier.

The IPC-9701A specification addresses how thermal expansion mismatch between the package and the PWB affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, PWB materials (e.g., FR-4), using a relatively larger nominal control thickness to minimize bending (0.093 in), surface finish choices to eliminate intermetallic failure (OSP, HASL), pad configuration to eliminate failure due to stress riser (non-solder mask defined or NSMD), and pad sizes having a realistic failure opportunity for package/PWB (80%–100% package pad), and so forth were standardized to minimize their effects on the test results.

The thermal cycle (TC) test ranges, test profile, and the number of cycles (NTC) reported were also standardized. These include the reference cycle in the range of 0 °C to 100 °C (TC1) and a severe military cycle condition of −55 °C to 125 °C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTC varied from a minimum value of 200 cycles to a reference value of 6000 cycles.

Three different thermal cycle profiles were used. Two of them are the same ranges as specified by IPC-9701A and the other one was specific to the NASA-JPL mission specific thermal cycle range requirement. These are:

1) Cycle A: The cycle A condition ranges from −50 °C to 75 °C with 2 °C to 5 °C/min heating/cooling rate. Dwells at the extreme temperatures are at least 10 min with a duration of 105 min for each cycle.
2) Cycle B: The cycle B condition ranges from −55 °C to 100 °C with 2 °C to 5 °C/min heating/cooling rate. Dwells at extreme temperatures are 30 min with a duration of 122 min.
3) Cycle C: The cycle C condition ranges from −55 °C to 125 °C with 2 °C to 5 °C/min heating/cooling rate. Dwells at extreme temperatures are at least 10 min with a duration of 159 min for each cycle.

The criteria for an open solder joint specified in IPC-9701 were used as guidelines to interpret electrical interruptions. For ceramic packages, once the first interruption was observed, many additional interruptions occurred within 10% of the cycle life. However, this was not the case for plastic packages. Opens were verified manually after removal from the chamber at the earliest convenient time.

X. Test Results

Fig. 4 shows optical photomicrographs of a CCGA assembly after 200 Cycle B (−55 °C/100 °C) thermal cycles. Even though no outright failures were observed, the CCGA solder joints showed some signs of damage which are more severe for the corner column joints. These test vehicles (TVs) were assembled using a stencil with 8 mil thickness whereas a number of other TVs were built using a mini-stencil with 10.5 mil thickness. Reductions in solder volume from its original state (solder loss) and solder appearance transition from smooth condition after assembly to graininess are other features of these solder joints. The two features that gradually occurred as the number of thermal cycles increased are clearly evident from the optical photomicrographs at 200 cycles. Fig. 5 shows scanning electron microscopy (SEM) of the solder joints before and after cross-sectioning. A large microcrack with a length of more than 50% of the solder joint length at the board side, signs of solder loss at its initiation site, as well as signs of microcracks in solder and at the interposer via on package side, are all apparent in Fig. 5.

Fig. 6 shows optical photomicrographs of both PBGA and CCGA 560 I/O assemblies after 2 937 Cycle A (−50 °C/75 °C)

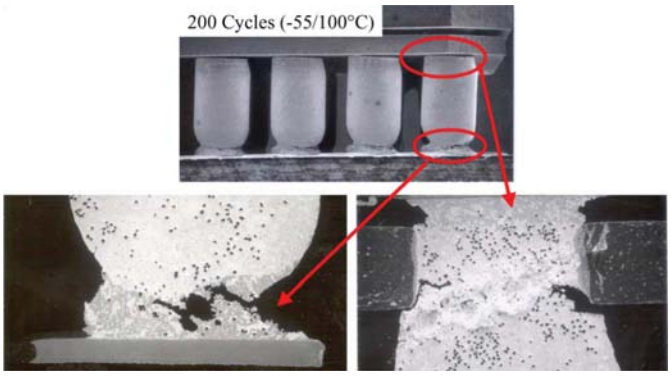

Fig. 5. SEM photomicrographs of CCGA built with 8 mil thick stencil after 200 cycles (−55 °C/100 °C). Note solder joint cracks from board and package at the interposer interface.

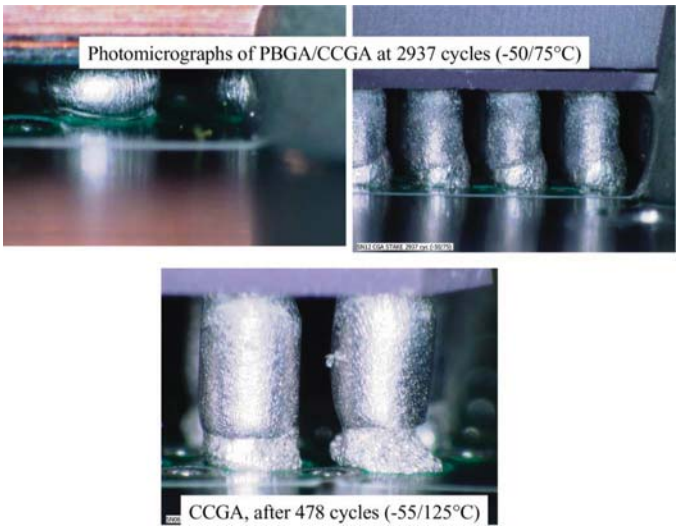

Fig. 6. Optical photomicrographs of PBGA and CCGA under two different thermal cycle conditions. Note graininess and solder loss for CCGA exposed at 125 °C. The CCGAs are assemble using with a 10.5 mil stencil thickness for paste printing.

and 478 Cycle C (−55 °C/125 °C) thermal cycles. As apparent, bulbous solder joints engulfing CCGA columns are formed due to using mini-stencil with 10.5 mil thickness for solder paste printing. For the maximum temperature of $(T_{\max})$ of 75 °C (Cycle A), there are no apparent degradation of CCGA and PBGA solder joints at 2 937 thermal cycles even though most of the assemblies have failed. The solder joint failures were from the package side within the package and interposer where they are hidden and therefore could not be inspected visually using optical microscope.

For the $T_{\max}$ of 125 °C (Cycle C), the joints at the board interface showed signs of insufficient solder with graininess contrary to its bulbous condition after assembly. To the best of the author's knowledge, this feature is not reported on in the literature and is a new finding. The solder feature changes with thermal cycling for the Cycle C condition are somewhat similar to the Cycle B condition with a $T_{\max}$ of 100 °C. On the other hand, the PBGA solder joints exposed to the same elevated maximum temperatures (100 °C and 125 °C) did not show signs of solder loss and graininess after identical number of thermal cycles.

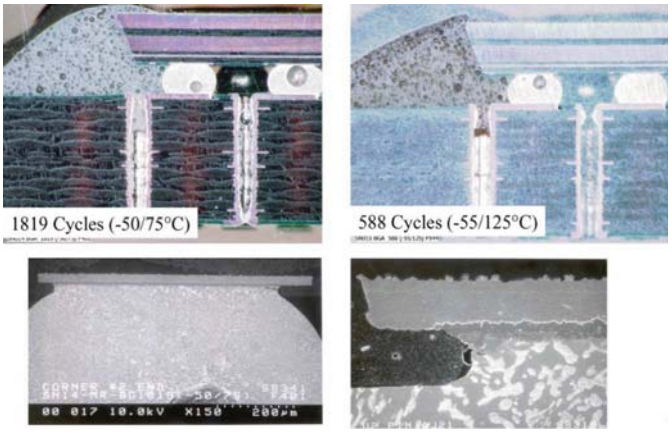

Fig. 7. SEM Photomicrographs before and after cross-section for PBGA package after 588 cycles (−55 °C/12 °C5).

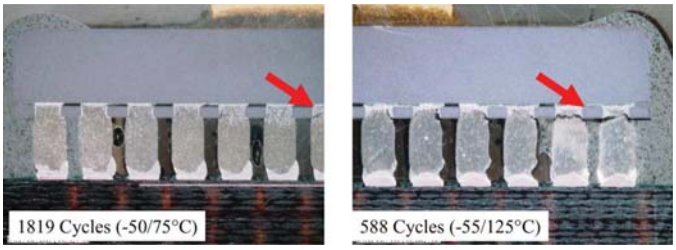

Fig. 8. Photomicrographs of column failure at interposer with corner staked over two thermal cycle ranges. Cracks locations are shown by arrow.

XI. Corner Staking Adhesive and Failure Mechanism Change

Fig. 7 compares optical and SEM photomicrographs of a PBGA assembly after exposure to 1 819 cycles in the range of −50 °C to 75 °C and the other one after exposure to 588 cycles in the range of −55 °C to 125 °C. Both assemblies had corner staking. For the $T_{\max}$ of 75 °C, no significant microstructural changes are apparent whereas for the $T_{\max}$ of 125 °C, a small microcrack was initiated in the solder joint at the package interface. The latter photo also clearly shows grain growth due to exposure to an elevated temperature. Similar optical photomicrographs for CCGA assemblies with corner staking after the same number of cycles and conditions [1819 (−55 °C/75 °C) and 588 (−55 °C/125 °C)] are shown in Fig. 8.

Although both CCGA assemblies had identical build processing parameters with identical corner staking materials and processes, the failure mechanisms were different and dependent on the temperature cycle range and the maximum temperature. One failed away from staking whereas the other (−55 °C/125 °C) failed within the staking adhesives at the interposer solder interconnection interfaces. To better understand microstructural evolution and the two failure mechanisms, further characterizations [17] were conducted using energy dispersive X-ray (EDX) and SEM to perform fractographic and metallographic analyses. Finite element simulation performed to map state of stresses/strains for assemblies with and without corner staking adhesive. CCGA Weibull failure data were analyzed and compared to other CCGA package types and presented in [18].

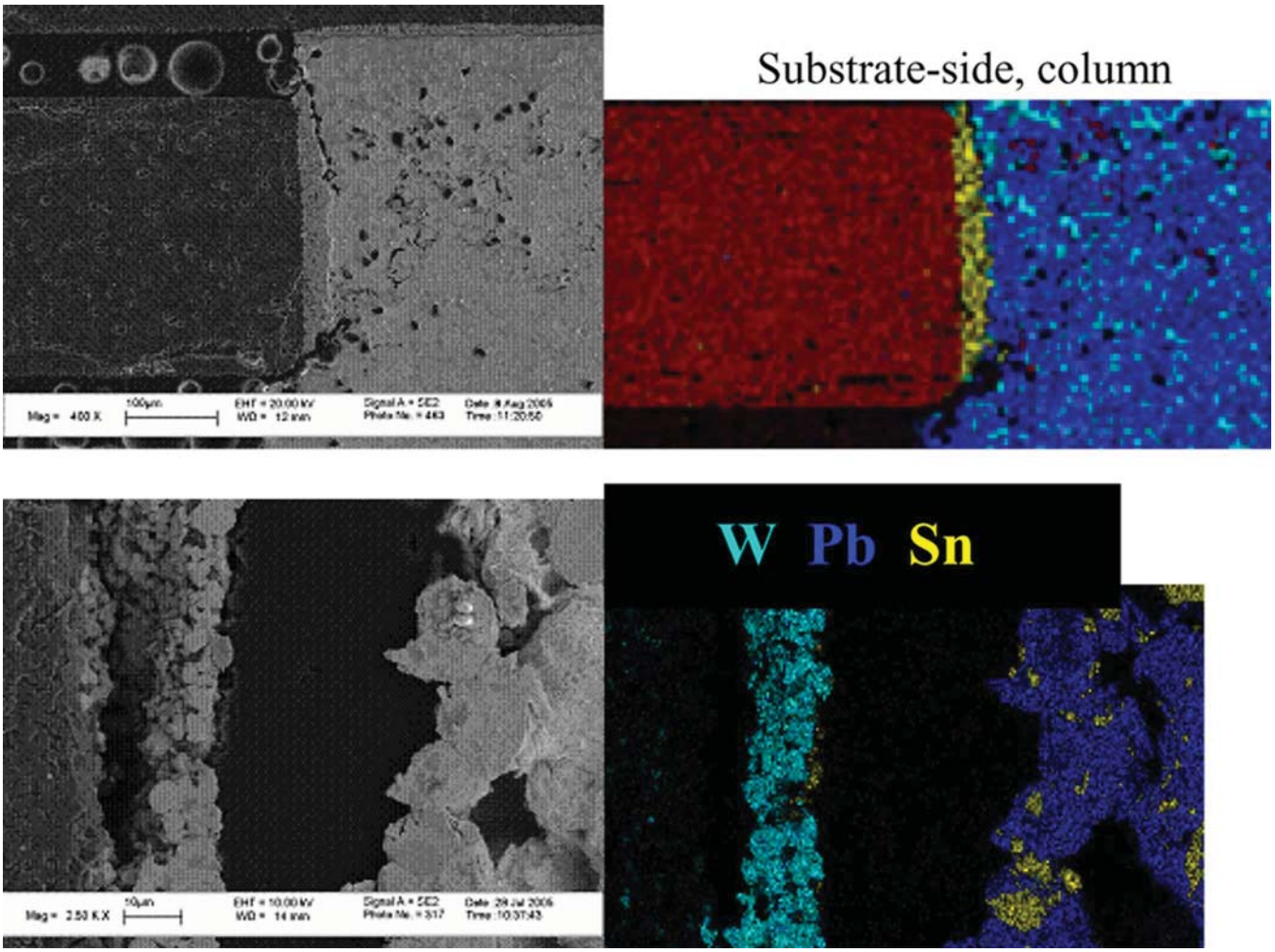

Fig. 9. CCGA solder joint crack on substrate side of (a) 50 °C/75 °C, and (b) −55 °C/125 °C TVs initiated from interposer/solder corner/fillet. EDX clearly reveals crack initiation and growth along the W-solder boundary.

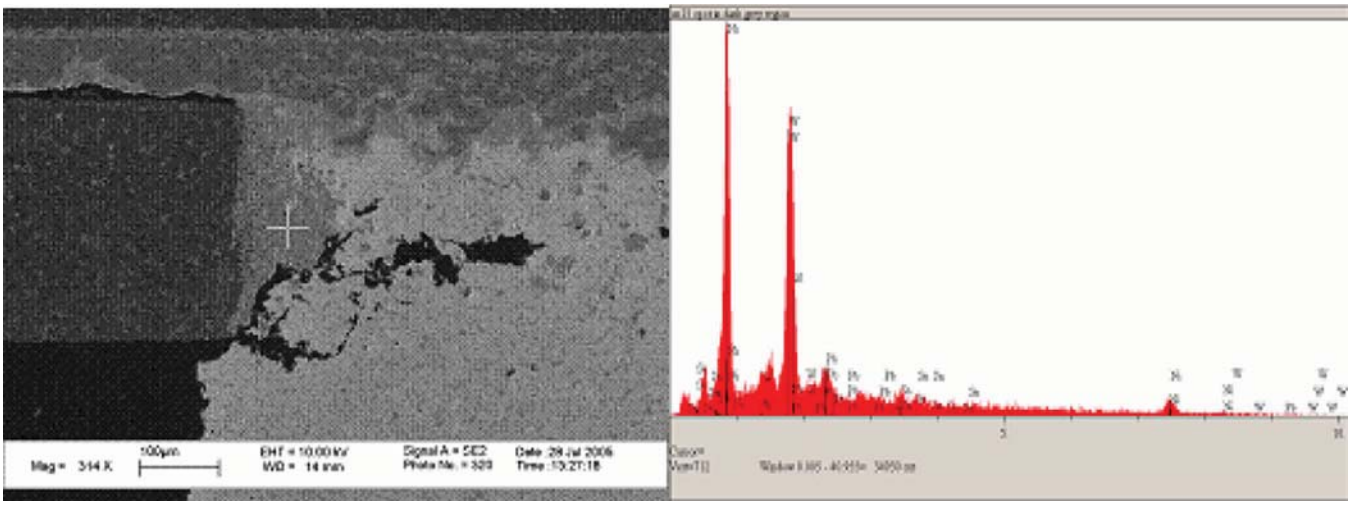

Fig. 10. Increased interposer metallization layer note (CCGA, −55 °C/125 °C, substrate side).

XII. EDX and Fracture Surface Morphology

EDX analysis showed that cracks were initiated from the interposer/solder fillet, and they grow along the interposer/solder interface before their transition into solder materials (see Fig. 9). Increased interposer metallization layer is noted for the column exposed to 125 °C, as shown in Fig. 10. Grain boundary cavitation indicative of creep mode of failure along a 45° angle to the column axis was also noted at the substrate side (see Fig. 11).

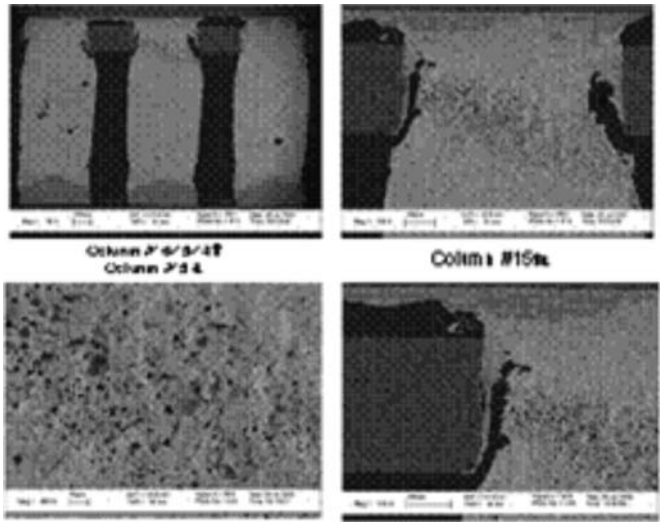

Fig. 11. Grain boundary cavitation noted on substrate side solder in −55 °C/125 °C ATC TV.

Also, Brittle intergranular cracking and solder loss were noted at the board side and near the staked package corners (see Fig. 12). The amount of solder loss was lower at the center columns with lower stresses and for the TVs exposed to 75 °C maximum temperature. This observation along with detection of solder loss along the Pb-rich and Sn-rich phase and grain boundaries detected using high magnification SEM/EDX analysis (Fig. 13), all indicate that solder loss occurs by grain boundary cracking due to brittle IMC and/or potential creep cavitation/coalescence, and eventual separation/loss.

XIII. Fracture Surface Morphology

Assemblies were pried open and the exposed fracture surfaces morphology were evaluated by SEM in order to investigate the mechanisms responsible for the solder cracking/failure. Fig. 13 shows fracture surface of solder joints on the substrate side, revealing an initial slow crack growth followed by unstable ductile failure for the TVs cycled in the range of −55 °C to 125 °C. A higher magnification SEM image of fracture surface showed the presence of striations, indicative of fatigue mode of solder failure.

Substrate side fracture surface of TVs exposed to lower maximum temperature cycle revealed somewhat a different morphology with smaller amount of fatigue and ductile failure zones and more of an intergranular failure. However, both samples showed intergranular morphology fracture surfaces with no indication of fatigue failure at the board side.

XIV. Finite Element Simulations

A finite element analysis model of the CCGA package assembly was created in ABAQUS to study the global deformation and stress fields induced due to thermal cycle test conditions. By virtue of the symmetry in geometry, loading and material properties, 28 307 quadratic hexahedron elements (type C3D20) and 146 931 nodes were used to model only half of the sample using proper symmetry boundary conditions (BC). Plastic properties were assigned only to the solder, while all other material are assumed to be hyper-elastic. The latter is the only material modeled as plastic and having temperature dependent properties. No creep rule was considered. The reflow temperature of 220 °C was taken as reference temperature for the stress-free configuration of the assembly. Only three saw-tooted thermal cycles were considered in simulation, alternating assembly between the minimum ($T_{\min}$) and $T_{\max}$ temperatures of one cycle. Two $T_{\max}$ cases were analyzed one for the 75 °C and the other one for the 125 °C temperature. During a thermal cycle the package experienced increasing stresses during cooling and stress relaxation in the heating phase.

Fig. 14 shows the stress field in the column interfaces at the end of the first and third cooling cycles for the 75 °C case. The first cooling induces the largest stresses. After two thermal cycles the intensity of the stresses is mitigated by the effect of the plastic deformation. This figure shows that, while the three corner columns are unloaded due to the polymeric stakes (not shown), the middle columns are subject to great stresses at the interfaces with the substrate (mostly) and the board. A similar scenario holds for the 125 °C case. Noticeable plastic deformation occurs in the solder due to load reversal and (kinematic) hardening.

The plastic shear strain fields which are critical for the creep and mode II cracking process are shown in Fig. 15 for both conditions (Cycle A and C). It is evident that the effect of the stakes is to shift the location of maximum shear strain from the corner columns with largest DNP (distance from neutral point) to the center columns. The results explain as why for the 75 °C case, the failure occurs in the center columns. However, the model seems to predict the same scenario also for the thermal cycle condition with the 125 °C maximum temperature. This discrepancy is a model limitation since the adhesive bond materials is modeled as hyper-elastic and the interfaces are perfect for such assumption.

The simulations show that stakes at the corners experience larger loads and higher plastic strains. Under these circumstances, the load-bearing capability of the reinforcements deteriorates rapidly at 125 °C and either cracks or cause significant creep deformation in the solder joints due to the large local stresses. Experimental phenomenology of Cycle C case confirms the occurrence of corner cracks and creep deformation. The glass-transition-temperature of staking material (T_g) may also contribute to this transition in load bearing capability, ifT_g is lower than 125 °C. Hardening and degradation of bonding polymer due to elevated temperature exposure are other factors that need to be considered in order to better project experimentally observed failure mechanism changes.

XV. Conclusion

It is well established that generally solder joint reliability of plastic packages on polymeric boards is better than that of their ceramic counterparts. This trend was verified through our investigation for the 560 I/O CCGA/PBGA packages with identical configuration. In addition, the effects of the following parameters are also identified.

1) Plastic package assemblies did not show failures to 2000 cycles whereas CCGA assemblies showed the first failure

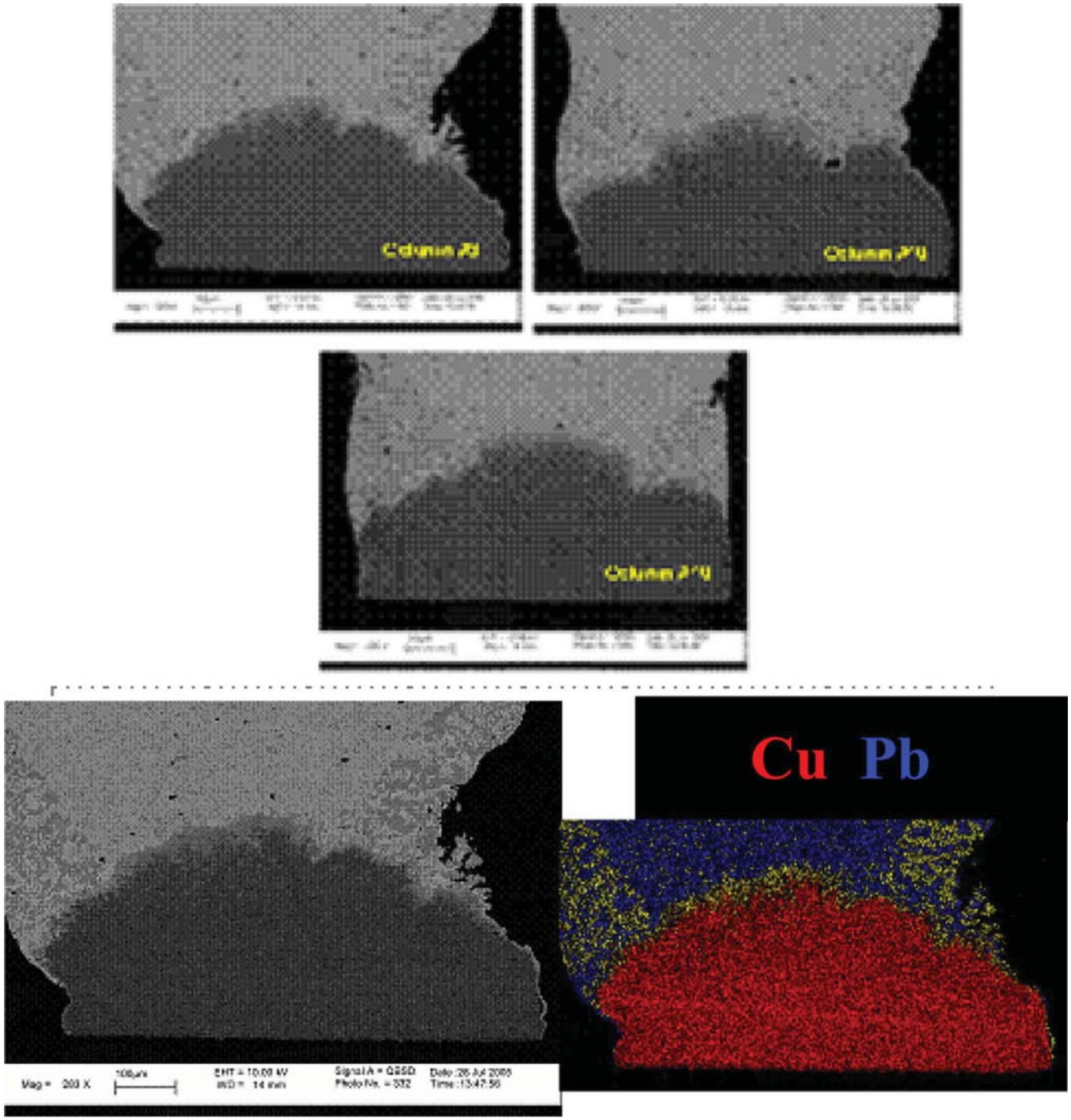

Fig. 12. Solder loss and Significant Cu inter-diffusion and IMC formation/growth was noted at board-side solder joints in −55 °C C ATC (much smaller growth for −50 °C C ATC).

at slightly above 1000 cycles when they were subjected to −50 °C/75 °C cycle.

2) Although the test data indicates good thermal cycling performance of PBGA assemblies over the widest thermal cycling range used, plastic package parts are not generally rated above 85 °C. For this PBGA, the package solder ball attachment did not meet pull strength requirement when subjected to isothermal aging at 125 °C for specific time as required for space application.
3) CCGA solder joints at the board interface, showed signs of graininess and solder loss when they were exposed to thermal cycling with a maximum temperature of either 100 °C or 125 °C. These changes were not observed for the PBGA solder joints or when CCGA assemblies were exposed to a 75 °C maximum temperature.
4) The PBGA assemblies with the corner staking adhesive showed no additional degradation or changes in failure mechanism compare to those without corner staking when subjected to thermal cycling to 2000 cycles.

The CCGA assembly with the corner staking; however, showed changes in failure mechanism. For −55 °C/125 °C cycle condition, failures were at the interposer interfaces of

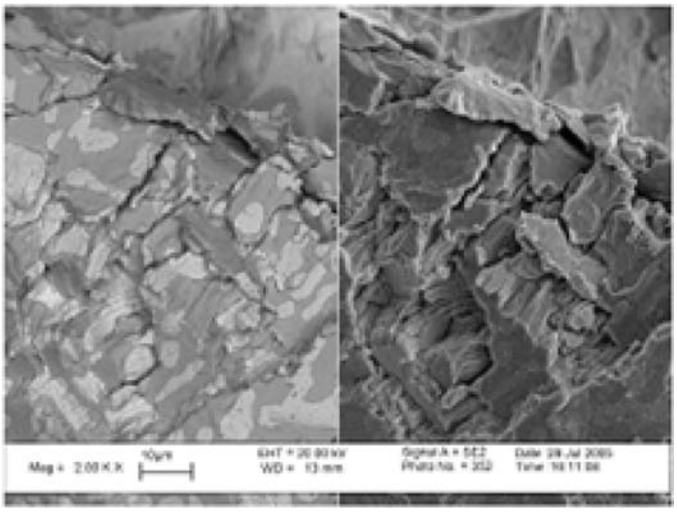

Fig. 13. Fracture surfaces of ATC tested (−55 °C) CCGA package, indicating fatigue failure at substrate-side of solder joints.

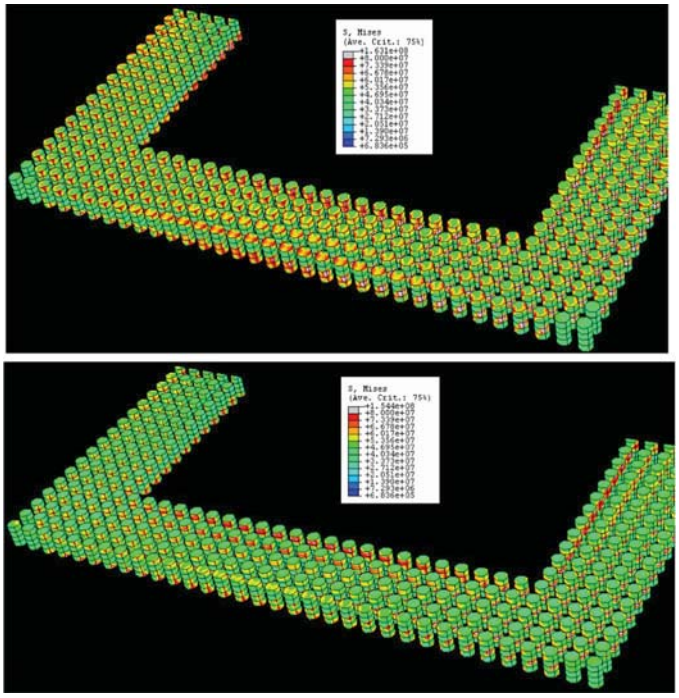

Fig. 14. State of stress in the solder columns for $T_{\max}$ of 75 °C after cooling to $T_{\min} = -55$ °C in the first (top) and third cycles (bottom).

those columns that were covered on by the adhesive. For −50 °C/75 °C cycle, failures were still at the interposer; however, they were from the center columns away from those covered by adhesive.

5) Finite element analysis projected stresses/strains increase at the center columns due to use of corner staking which is partially in agreement with experimental results. Further refinement in modeling simulation is required to be implemented in order to be able to project experimentally observed failure mechanism changes due to maximum temperatures in thermal cycling.

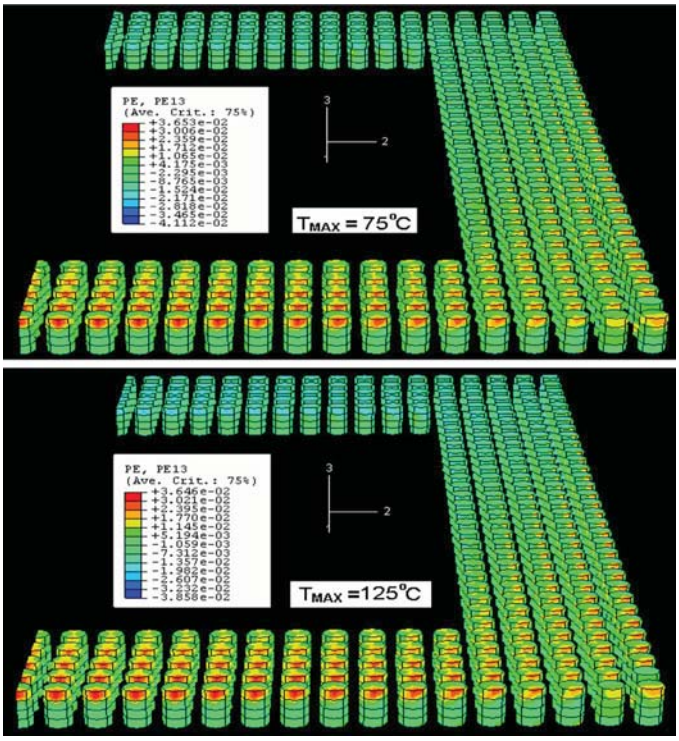

Fig. 15. Distribution of the ε_{13} component of the plastic strain for $T_{\max}$ of 75 °C and 125 °C, the distributions look very similar.

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